OPINION: *The future of rugged COTS*

Daily Briefing: *News Snippets*

Military EMBEDDED SYSTEMS

VOLUME 6 NUMBER 7
OCTOBER 2010

INCLUDING:

Chris A. Ciufo
"Neighborhood watch" for CPUs

Field Intelligence
Military moves to AdvancedTCA

Mil Tech Insider
Is write-once SW in our future?

Legacy Software Migration
Wind River:
Hypervisors speed A&D migration

MIL-EMBEDDED.COM

Full-motion video shows battlefield's ebb and flow

ARINC 661 visualizes standard cockpit displays

Also:
OpenVPX's ecosystem

Innovation sets us apart

Avionics Databus Test, Simulation & Embedded Solutions

Lightweight, small, rugged, reliable, feature rich and cost-effective. These are only a few of the benefits of the new AB2000 series of Avionics BusBoxes® from Ballard Technology. They deliver outstanding avionics performance with multi-protocol and flexible expansion capabilities. Conductively cooled, the AB2000 is ideal for rugged avionics applications such as serving and recording data, converting protocols and providing federated control. Find out today how AB2000 innovation can work for you.

The AB2000 offers multi-protocols in a single, lightweight rugged format.

ARINC 429
MIL-STD-1553
Ethernet
RS232/422
Digital I/O
USB

Innovation for your success

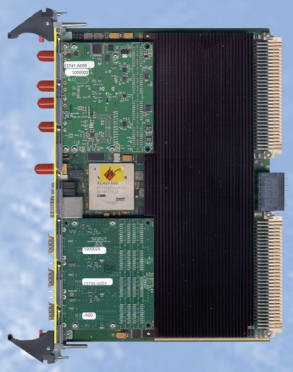
For more information call 425.339.0281 or visit us at www.ballardtech.com

Ballard TECHNOLOGY

Annapolis Micro Systems

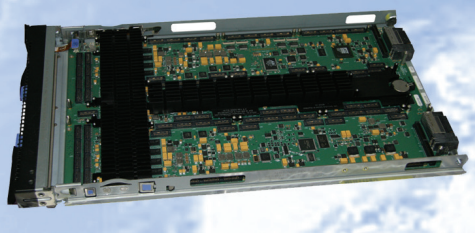
The FPGA Systems Performance Leader

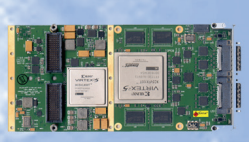
High Performance Signal and Data Processing in Scalable FPGA Computing Fabric

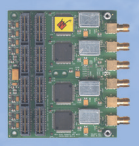


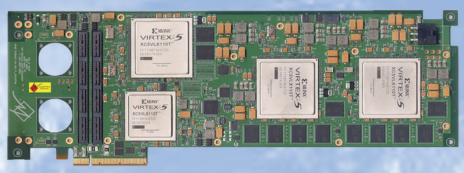
GEOINT, Ground Stations, SDR, Radar, Sigint, COMINT, ELINT, DSP, Network Analysis, Encryption, Image Processing, Pattern Matching, Oil & Gas Exploration, Financial Algorithms, Genomic Algorithms

Direct Seamless Connections with no Data Reduction
Between External Sensors and FPGAs
Between FPGAs and Processors over IB or 10GE
Between FPGAs and Standard Output Modules
Between FPGAs and Storage Arrays









Annapolis Micro Systems

Ultimate Modularity
From 1 to 8 Virtex 4, 5 or 6 FPGA/Memory Modules
Input/Output Modules Include:
Quad 130 MSPS thru Quad 550 MSPS A/D
1.5 GSps thru 5.0 GSps A/D, Quad 600 MSps D/A,
Dual 1.5 GSps thru 4.0 GSps D/A
Infiniband, 10G, 40G or 100G Ethernet or SFPDP

VME/VXS/VPX, IBM Blade, PCI-X/PCI Express, PMC/XMC, MicroTCA

No Other FPGA Board Vendor Streams This Volume of Data Real Time Straight Into the Heart of the Processing Elements and Then Straight Back Out Again

190 Admiral Cochrane Drive, Suite 130, Annapolis, Maryland USA 21401
wfinfo@annapmicro.com USA (410) 841-2514 www.annapmicro.com

Military EMBEDDED SYSTEMS

October 2010 Volume 6 Number 7

COLUMNS

DEPARTMENTS

ON THE COVER:
A U.S. "Liberty" cargo ship (U.S. MARAD, circa 1941/'42) recalls the days during World War II when neither the Allies nor the Axis precisely knew where the battlefield was. Huge swaths of the North Atlantic between North America and Europe were undetectable by opposing forces. Today, battlefield video from UAV/UAS platforms supplements satellite imagery, making it difficult for adversaries to hide – even on the open ocean. [Image courtesy of: Library of Congress; U.S. Office of War Information, Overseas Picture Division, Washington Division]

Published by: OpenSystems media.

ISSN: Print 1557-3222

WEB RESOURCES

Subscribe to the magazine or E-letter
Live industry news • Submit new products
http://submit.opensystemsmedia.com

White papers:
Read: http://whitepapers.opensystemsmedia.com
Submit: http://submit.opensystemsmedia.com

Mission Critical

Make the Dreamliner a reality

Breakthrough dependability

Boeing 787 Dreamliner
The Wind River VxWorks platform proved instrumental in the development of the Boeing 787 Dreamliner—history's fastest selling wide-body aircraft.

Wind River embedded systems deliver the cutting-edge reliability and performance that fuel innovation.

Boeing's 787 Dreamliner is taking flight with an innovative integrated modular avionics (IMA)-based Common Core System (CCS) developed by GE Aviation and enabled by Wind River.

Our industry-leading VxWorks 653 partitioning operating system is the foundation for GE's CCS, which serves as the Dreamliner's central nervous system by infallibly orchestrating the operation of over 70 applications supplied by over 15 Boeing suppliers.

VxWorks enables the asynchronous integration of multiple suppliers and allows for applications of different RTCA DO-178B safety criticality levels to reliably run on a single shared computer platform.

It's the kind of cutting-edge dependability and proven performance that's made Wind River a trusted leading provider of advanced embedded solutions for aerospace and defense.

Take your innovation to new heights. Contact us today for our Mission Critical Toolkit, now available for a limited time at www.windriver.com/missioncritical/safety.

WIND RIVER

ADVERTISER INFORMATION

Page	Advertiser/Ad title
18	**ACCES I/O Products, Inc.** – USB embedded I/O solutions
57	**AdaCore Technologies** – Safety, security, reliability
3	**Annapolis Micro Systems, Inc.** – High performance signal and data processing
47 MCD	**Annapolis Micro Systems, Inc.** – High performance signal and data processing
40	**Avnet Electronics Marketing** – Avnet enables higher levels of integration
2	**Ballard Technology** – Innovation sets us apart
22	**CoreSolid Storage** – XDOM mini PCI Express DiskOnModule
60	**Curtiss-Wright Controls Embedded Computing** – Defy size, weight and power
38	**Curtiss-Wright Controls Embedded Computing** – VPX6-187
38	**Curtiss-Wright Controls Embedded Computing** – MPMC-9351
38	**Curtiss-Wright Controls Embedded Computing** – VPX3-685
38	**Curtiss-Wright Controls Embedded Computing** – CHAMP-AV6
21	**Data Device Corporation** – New MIL-STD-1553 test cards
7	**D-TA Systems** – 10 Gigabit sensor processing
43 MCD	**D-TA Systems** – 10G series record and playback systems
45 MCD	**Elma Electronic** – Digital printing for 19" front panels
38	**Elma Electronic** – OpenVPX Backplane & Accessory Family
37	**Elma Electronic** – Cabinets for rugged, seismic and mobile applications
24	**Elma Electronic – Systems** – Embedded storage for secure data
27	**Excalibur Systems, Inc.** – Dragon
53 MCD	**Excalibur Systems, Inc.** – Dense?
59	**GE Intelligent Platforms, Inc.** – You can only target what you can track
13	**Hartmann Elektronik** – VME backplanes from the experts
50 MCD	**Hartmann Elektronik** – System platform
38	**Hartmann Elektronik** – 3U VPX Backplane
39	**InnoDisk** – EverGreen
45 MCD	**Interface Concept** – Switches and IP routers
51 MCD	**Kontron** – OM6061
31	**LCR Electronics** – Engineered for your application
56	**Magma** – Bridge telecom to legacy platforms
51 MCD	**MEN Micro Elektronik GmbH** – The future of CompactPCI is serial
55	**Microhard Systems, Inc.** – Wireless innovation
10, 11	**Microsemi** – We create space
49 MCD	**N.A.T. GmbH** – Innovation in communication
32	**Nallatech** – FPGA accelerated computing
36	**North Atlantic Industries** – Multifunction I/O boards
13	**Parvus Corporation** – Qualified to perform
19	**Pentek, Inc.** – Stroke of genius
33	**Phoenix International** – RPC12 ruggedized 3U Fibre Channel RAID system
52 MCD	**RadiSys Corporation** – From theoretical to mission-critical
42 MCD	**RightHand Technologies** – COM Express improves time-to-market for embedded computing
33	**Sanmina-SCI** – Viking Modular Solutions
49 MCD	**Sanmina-SCI** – Viking Modular Solutions
46 MCD	**Schroff, a brand of Pentair Electronic Packaging** – Need to match price and performance
29	**Schroff, a brand of Pentair Electronic Packaging** – Schroff understands the demands
48 MCD	**TEWS Technologies LLC** – I/O solutions for MicroTCA/ATCA
55	**TEWS Technologies LLC** – COTS I/O solutions
17	**Trident Space & Defense** – Proteus Series SSDs
25	**Tri-M Systems Inc.** – PC/104 Can-Tainer
35	**Tri-M Systems Inc.** – 100MHz PC/104 module
54 MCD	**Vector Electronics & Technology, Inc.** – VME/cPCI ruggedized chassis
5	**Wind River Aerospace & Defense Division** – Mission critical
28	**Z Microsystems, Inc.** – Rugged rack mounted servers

OpenSystems media

Military EMBEDDED SYSTEMS

DSP-FPGA.com | VME and Critical Systems | PC/104 and small form factors THE JOURNAL of MODULAR EMBEDDED DESIGN

INDUSTRIAL EMBEDDED SYSTEMS | CompactPCI Advanced & Micro TCA SYSTEMS | Embedded COMPUTING DESIGN

Editorial/Business Office

16626 E. Avenue of the Fountains, Ste. 203
Fountain Hills, AZ 85268
Tel: 480-967-5581 ■ Fax: 480-837-6466
Website: www.opensystemsmedia.com

Publishers: John Black, Michael Hopper, Wayne Kristoff

Vice President Editorial: Rosemary Kristoff

Vice President Marketing & Sales:
Patrick Hopper
phopper@opensystemsmedia.com

Business Manager: Karen Layman

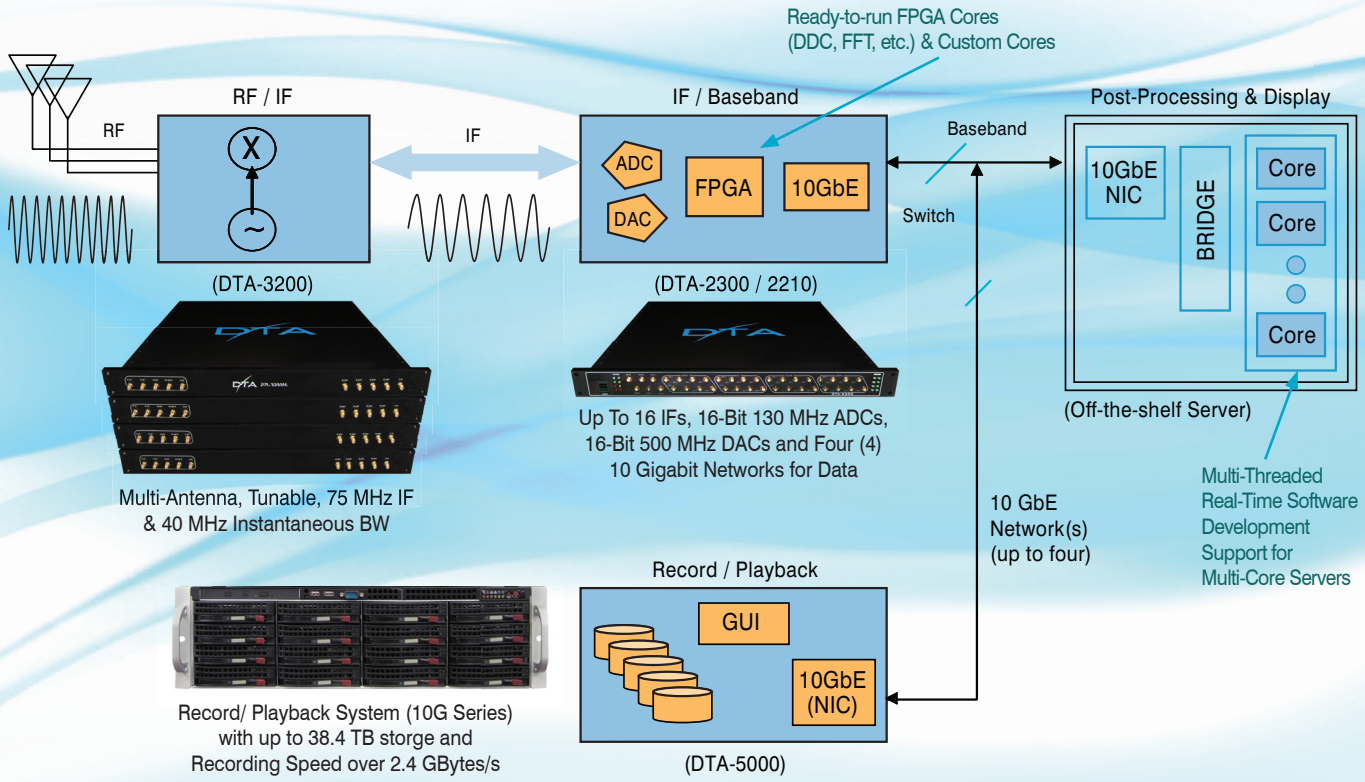
10 GIGABIT SENSOR PROCESSING... WELCOME ABOARD!

Whatever your application...

Phased Array Radar, SIGINT, ELINT, SATCOM, HF/VHF/UHF Radio, MIMO, Cognitive Radio, Wireless Basestation, Sonobuoy, RF Test & Simulation

...We have you covered from RF to Baseband to Multi-Core Software Processing.

D-TA's solutions drastically reduce deployment time & cost.



We have pushed the envelope in every direction to simplify your development effort.

Let's get started!

1-877-382-3222
SALES@D-TA.COM
WWW.D-TA.COM

NOTHING ELSE COMES CLOSE

D-TA SYSTEMS INC.
A Sensor Interface and Processing Company

SENSOR PROCESSORS THAT DRASTICALLY REDUCE DEPLOYMENT TIME AND COSTS

Field Intelligence

Military moves applications to Advanced Telecommunications Computing Architecture

By Duncan Young

The Advanced Telecommunications Computing Architecture (AdvancedTCA) was developed as an embeddable computing architecture to provide a wide variety of digital voice and data services with future expansion capability, plus 5-nines (99.999 percent) reliability. It offers an architecture optimized for highly data-intensive applications based on IP and Ethernet. AdvancedTCA's extended 8U form factor of 11.02 x 12.68 inches (280 x 322.25 mm) is larger than equivalent VME or VPX modules, giving the space and thermal characteristics needed for high-end, server-class performance on a single blade. This makes it an ideal platform to host large, cooperative, shared applications across many locations with many users such as air traffic control, battlefield command, C4ISR surveillance systems, and naval combat systems, potentially displacing many less reliable commercial-based solutions.

IP-centric architecture

Despite very effective continuous improvement programs lasting a decade or more, many existing 6U VME- or CompactPCI-based systems have reached the limits of their architectural capability and are now due for major upgrade or replacement. During this time, AdvancedTCA appeared to have been sidelined by military systems integrators, yet many of the values of military users and telcos are convergent: reliability, longevity of supply and support, scalability, and upgradeability. However, now AdvancedTCA's IP-centric architecture and massive performance potential have made it a serious contender for next-generation surveillance and combat systems in the protected environments of naval submarine and surface warships or wide-bodied aircraft such as the new P-8 Poseidon multimission, antisubmarine warfare aircraft.

AdvancedTCA's application space

But do not expect to see rugged, conduction-cooled AdvancedTCA compete with VPX (VITA 46) or VPX-REDI (VITA 48) anytime soon. The extended 8U PICMG 3.0 blade form factor would require considerable stiffening plus mechanical separation into smaller areas to keep vibration resonances outside the specified ranges for rugged equipment. Power dissipation of >250 W per slot will also demand more exotic cooling regimes such as air or liquid flow-through. AdvancedTCA's application space is in benign or protected environments and its real strength for this market lies in its consistent and well-defined infrastructure, offering real plug-and-play between products and vendors at all levels. Intelligent Platform Management Interface (IPMI) provides shelf management and hot-swap capabilities using predefined Ethernet channels, while fabrics or networks such as InfiniBand or 10 GbE plus their switches have predefined slots and configurations for ease of integration. Using primarily Intel-based processors, AdvancedTCA is well supported with industry-standard operating systems such as Linux and Windows.

IP-based sensor processing

Large cooperative systems and applications shared among many users use IP for communication and data distribution between nodes. The raw data rates of most sensor types such as sonar (hull-mounted, towed, and dipping), Electro-Optical (EO), signals intelligence, and radar allow for compression and packetization at the sensor for downstream processing, often distributed throughout a system or network of systems. Packets can be streamed from sensors to wherever they are required: for display as raw images, for processing into tracks and targets, to fuse together sensor images, or to collate multiple sensor inputs into a tactical battlespace display.

Generally, AdvancedTCA has three blade types: fabric switch, processor, and I/O. Processor and I/O blades use Advanced Mezzanine Card (AMC) modules to add functionality and connectivity such as external network ports or packet processors. The 8U size of an AdvancedTCA blade is capable of supporting multiple server-class processor devices. An example of this is the A10200 SBC from GE Intelligent Platforms with dual Intel Xeon NEBS-certified 5600/5500 quad- and six-core processors running at 2 GHz, plus 64 GB of DDR3 SDRAM (Figure 1).

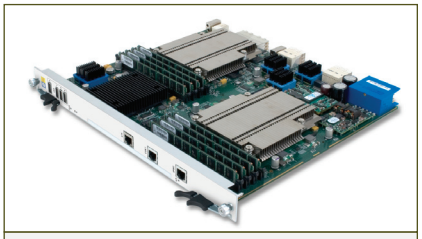


Figure 1 | The A10200 dual Xeon AdvancedTCA SBC from GE Intelligent Platforms

Network enabled battlefield vision

AdvancedTCA's success in the telecommunications industry can be applied directly to the future network enabled battlefield, where the Army's vision is for every soldier to have secure, 4G cell phone-like functionality. This will offer streaming video via personal, local, and remote sensors, plus access to real-time analytical and tactical planning services, GPS, maps, voice, text, data, and training exercises. As well as the network infrastructure required to support such services, the demands of security will render some additionally challenging dimensions:

- Maintaining service in high-EMI environments
- Setting and sustaining security levels and access controls for streaming video throughout the network and across national boundaries without introducing undue delays
- Protecting content with encryption
- Protecting the network against attack

AdvancedTCA – with its proven track record, functionality, and processing capability – can play a significant role in this network enabled battlefield vision.

To learn more, e-mail Duncan at duncan_young1@sky.com.

Mil Tech Insider

The promise of Open APIs: Is write-once software in our future?

By Steve Edwards

Time to deployment is a key driving force in the embedded military market. The faster advanced technology is delivered to the field to support the warfighter and save lives, the better. The COTS approach has significantly helped in speeding the delivery of commercial hardware and in furthering open-standards body efforts. For example, the recent OpenVPX/VITA 65 work will help cut development time for high-performance embedded systems. Now, the embedded military market is poised to take the next big leap in improving time to deployment through the adoption of Open APIs to speed system application development. Open APIs can ease heterogeneous hardware technology integration, drastically cutting time, cost, and complexity for building larger multimode systems.

OpenFabrics tackles heterogeneous systems

Today, embedded system integrators must deal with myriad fabric choices – such as PCI Express, Serial RapidIO, Ethernet, and InfiniBand – and a wide variety of processors such as Intel, Power Architecture, GPGPUs, and FPGAs. Getting data to move back and forth efficiently between these various processors and fabrics within a fixed Size, Weight, and Power (SWaP) envelope is a daunting task. Initiatives in the commercial market are underway to address the challenge of integrating heterogeneous systems. One such initiative, led by the OpenFabrics Alliance (www.openfabrics.org) has developed a middleware stack, known as the *OpenFabrics Enterprise Distribution* (OFED). The key component of this open source initiative is OpenFabric User VERBS (OF-UV)-enabled software, such as OpenMPI, that communicates through the VERBS API layer, the OS, the BSP, and the fabric. OpenFabrics supports Windows, Linux, OpenSolaris, and 10 GbE and InfiniBand. It enables the programmer to code without concern for which OSs or fabrics the system hardware is based on.

Getting to "write-once" software

The embedded community should consider this approach. Proprietary APIs typically only support hardware supplied by the API vendor, and it is difficult to adapt to hardware from other manufacturers. Open APIs are agnostic to fabric, processor, or the system at the board level. The user program writes to middleware that is abstracted to a layer from which the middleware talks to the hardware. This means software can be developed earlier, without having to wait for the target hardware to become available. The promise is that software is written once, but scales with the underlying technology without needing to be rewritten as the number of cores grows and the fabrics evolve from, for example, 10 Gbps today to 100 Gbps within four years.

Multicore drives software complexity

The increased use of multicore processors is driving embedded integrators to use ever more complex software. Flat memory model real-time OS development will become less common for the most sophisticated applications. Mil/aero signal processing applications are turning to multicore processors, with faster and greater quantities of memory and greater bandwidth requirements. By using commercial abstraction software via Open APIs, developers will not have to optimize their code to the byte level. Processors are becoming fast enough to meet many latency requirements without needing to provide "perfect real time"; "near real time" will frequently suffice. One indication is that some customers are now deploying radar systems based on Windows XP that would have been unheard of a decade ago.

The MCAPI initiative

Another Open API initiative is Multicore Communication API (MCAPI), led by the Multicore Association (www.multicore-association.org/home.php). This group is working to maximize the efficiency of embedded applications as they are distributed across multiple heterogeneous boards. The MCAPI is in the early stages, and its 1.0 spec is expected to be completed by the end of this year.

As an embedded community, we are just beginning to engage in the Open API endeavor. In a perfect world, one could leverage all the fruits of the commercial market, but the SWaP requirements demand specialized components that will likely limit adoption. Mapping applications to Open APIs is a trade-off. Running open-standards middleware requires a design sacrifice of some memory, bandwidth, and processor speed as more complexity is added in the data transport, OS, and middleware.

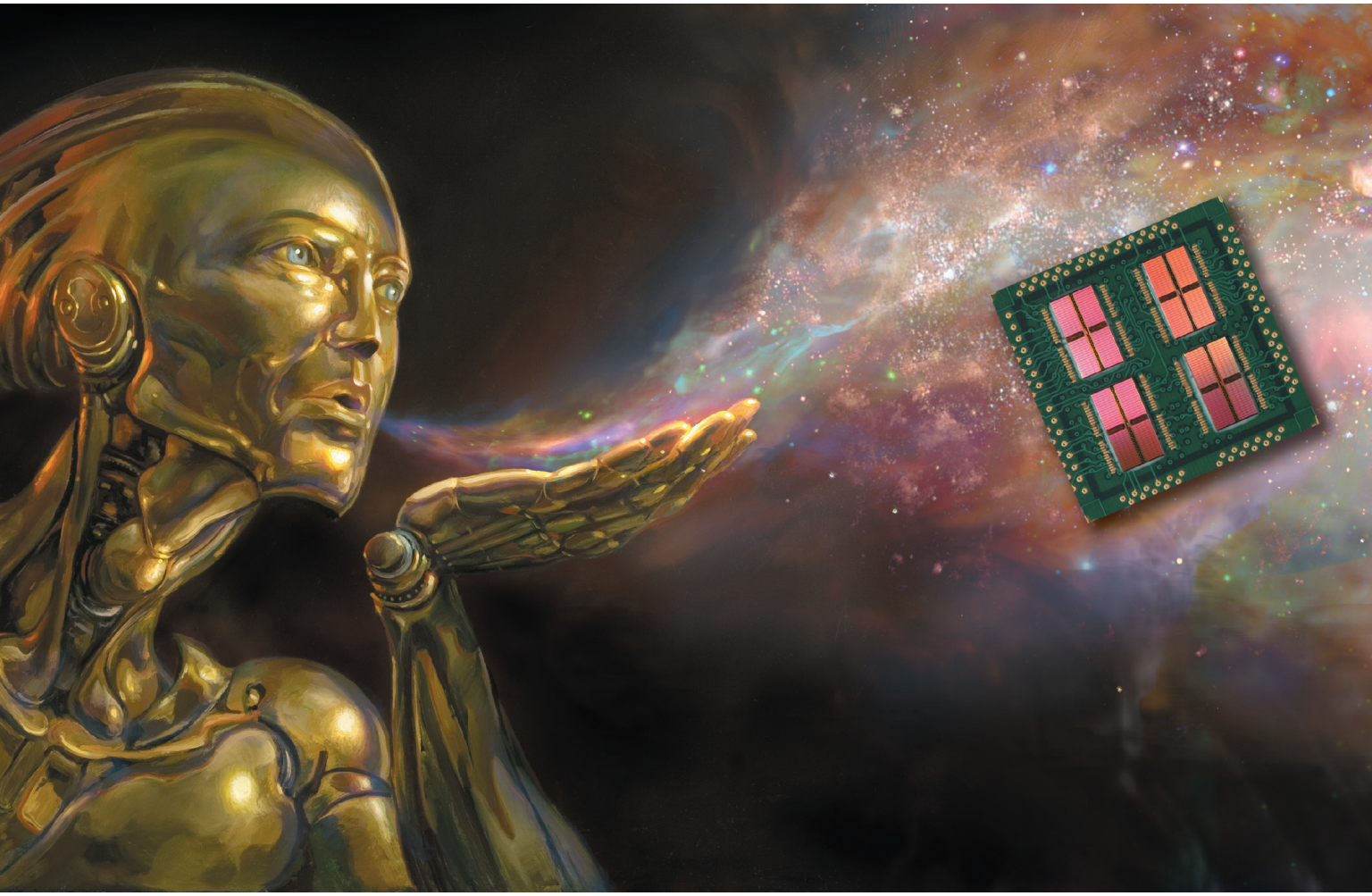
Speeding deployment with Open APIs

Embedded military vendors are now seeing increased interest from military market customers for high-level middleware support, such as Distributed Distribution Service (DDS), OpenMPI, and VSIPL++, which combines a math library function with a data transport. With Open APIs, customers see the potential to decrease their time to deployable product by getting development started earlier. They can also leverage data transport abstraction to run on the actual embedded system later in the development cycle.

At Curtiss-Wright, for example, we plan to contribute and support these Open APIs on our rugged hardware while optimizing the total system SWaP, enabling mil/aero customers to develop and deploy more rapidly. To ensure that the military COTS community can optimize its use of these burgeoning Open API standards efforts – and that its unique market requirements are heard and understood as these standards are developed – the embedded board and subsystem community should support the MCAPI and OpenFabrics initiatives. Increased communication and involvement among the embedded industry, competitors, customers, and these open source software groups could benefit us all.

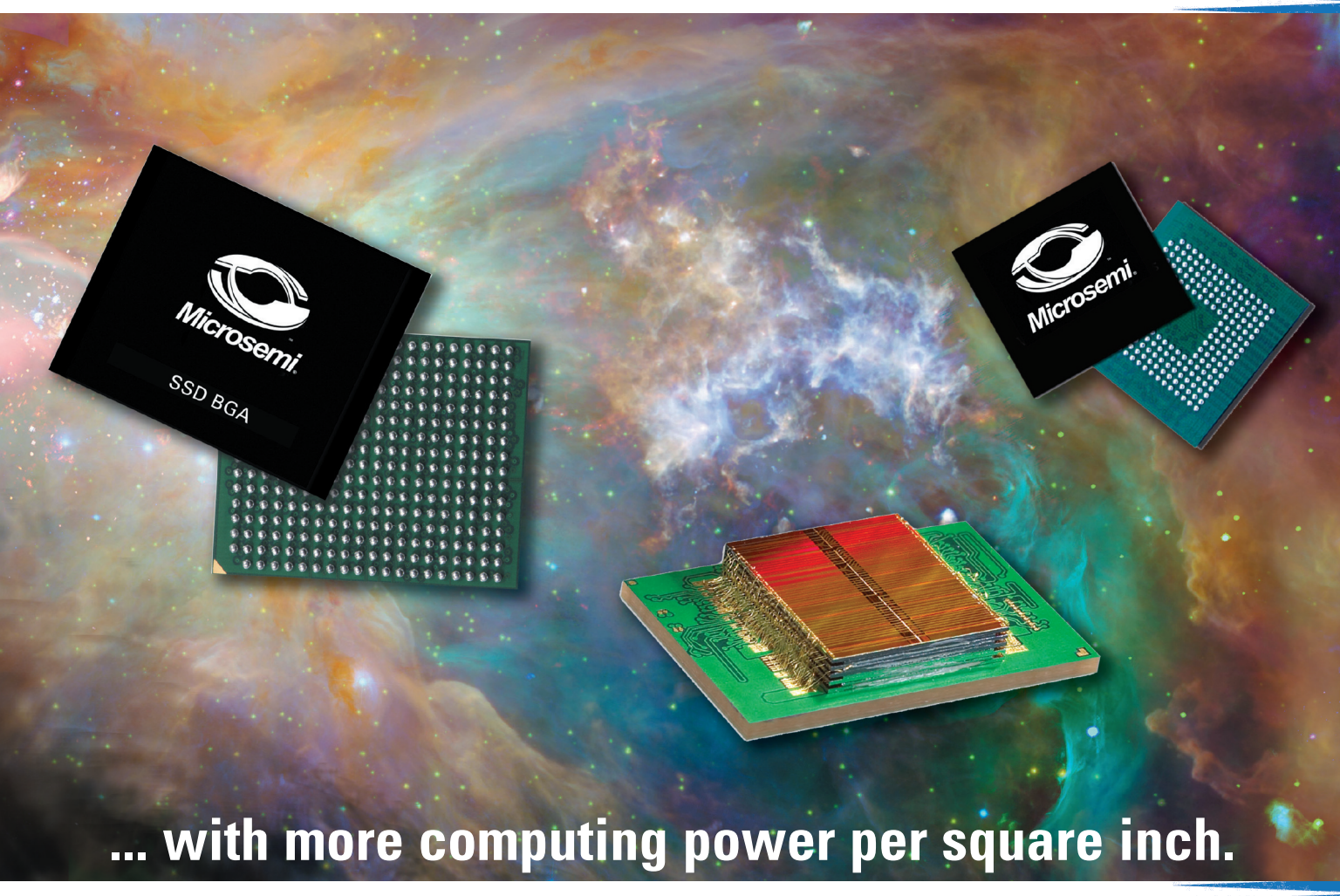
To learn more, e-mail Steve at Steve.Edwards@curtisswright.com.

We create space…



Microsemi's lean microelectronic solutions increase board density, solve component incompatibilities, reduce design complexity, and extend product life and environmental performance in military applications. We offer turnkey design, assembly and test of custom multi-chip solutions, and a wide range of standard military off-the-shelf space-saving solutions.

Expand the possibilities; visit **www.whiteedc.com/spacesaving.**



... with more computing power per square inch.

Our SLC NAND flash SSD BGA provides big features in a miniaturized package, freeing up precious board space. It is engineered specifically for the defense market, designed to ensure data reliability in mission critical rugged and mobile systems. Constructed using a 32-bit RISC processor as its core storage controller, this SSD is available in 4, 8 and 16 GByte densities.

Learn more at **www.whiteedc.com/ssd.**

602.437.1520 TEL | 602.437.9120 FAX

Microsemi

Securing the Future Through the Power of Design

WWW.WHITEEDC.COM

Legacy Software Migration

By Chip Downing

Next-generation multicore hypervisors accelerate legacy software migration in A&D systems

The challenge of maintaining deployed systems in Aerospace and Defense (A&D) can span long life cycles that integrate legacy platforms with new capabilities, while continuing to drive down Size, Weight, and Power (SWaP) demands. Deploying systems based upon advanced multicore processors executing mixed OS and hypervisor environments is an effective strategy to bridge existing assets into future platforms, while consolidating environments into smaller system footprint frameworks.

There is an unstoppable trend in aerospace and defense systems to move to more advanced multicore silicon platforms that feature more processing power than legacy technologies. This not only enables a dramatic reduction in SWaP, but it also – when combined with advanced operating environments – can enable a new generation of systems that can easily endure technology refresh cycles with significantly less testing. These technologies also now contain multiple OS environments, like VxWorks and Linux, to enable even greater scalability and economy over traditional platforms.

This is a significant departure from existing single core, single OS systems. It requires increased awareness of both underlying processor boards and peripherals, interaction of the cores, and supported OSs. A multicore platform will share more system resources (like interrupt controllers, devices, and caches) than single core and traditional multiprocessor environments. Therefore, these systems' configuration and deployment require more focus on the system design. Efficient embedded hypervisors, hosting diverse guest OSs and controlling allocation and utilization of individual cores, offer a compelling choice in abstracting away a significant element of risk in next-generation programs.

Enabling legacy in next-generation systems

One of the biggest challenges of migrating legacy applications into future systems is combining these applications with newer operating environments. Although this can be accomplished with AMP and SMP multicore configurations, an efficient embedded hypervisor not only allows these applications to be moved into the future, but it also enables a smaller platform footprint. This creates an efficient forward-looking design that can easily sustain a hardware refresh cycle.

A multicore embedded hypervisor is the only platform that can truly enable rapid technology refresh. By abstracting away the exact hardware environment, system designers can now move from a four-core multicore system to an eight-core platform of the same silicon family without forcing a complete retest of all applications. Let's take a closesr look at these ideas.

Next-generation platform choices

There are three basic configuration options for multicore systems:

1. AMP – Asymmetric multiprocessing configurations, where each core has a separate instance of an OS.
2. SMP – Symmetric multiprocessing configurations, where one operating system controls access to all or a set of processor cores. Allocation of tasks/threads to a specific core, along with communication between threads/tasks running on separate cores, is managed by the SMP OS.
3. Embedded hypervisor – The most flexible method for configuring multicore systems is to employ a hypervisor that abstracts away the underlying hardware environment and controls partitioning of all processor cores and peripherals on the board.

Embedded hypervisors are a thin layer of code that partitions hardware into virtual environments (referred to as "virtual boards") and the OS inside these virtual boards. Virtual boards run in separate address spaces [protected by the Memory Management Unit (MMU)]. A virtual board that can run on a single core can run SMP across multiple cores, or can be scheduled with other virtual boards on a single core on either a priority preemptive or time-based schedule. This is accomplished by virtualizing or partitioning key components of a system:

- CPU – By virtualizing the CPU, one can either share a single core with multiple virtual boards on top of one physical processing core or dedicate a single core or a set of cores to a single virtual board.
- Memory – Memory virtualization involves partitioning the physical memory so multiple partitions can use parts of the real memory. This allows more efficient memory use and creates an abstraction layer for separating and controlling memory access.
- Devices – Devices can either be partitioned (dedicated to a single virtual board) or virtualized and shared between multiple virtual boards.

Selecting the optimal hypervisor

Many different types of hypervisors are available, and the most well known are full-featured IT hypervisors such as VMware, KVM, and Xen. These hypervisors abstract physical hardware and offer comprehensive features such as remote management, load balancing, and failover. But these features require expensive scheduling algorithms, making them unsuitable for small, real-time, deterministic embedded systems, which need a thin, small hypervisor that maintains the RTOS's real-time capabilities and determinism in these environments. Embedded hypervisors – such as the Wind River Hypervisor or

VxWorks MILS Separation Kernel (SK) – are optimized for performance, isolation, and certification.

Moreover, three key capabilities exist for hypervisor technology in the A&D market:

1. Ease of migration of legacy applications and operating environments into new platforms.
2. The ability to reduce SWaP by consolidating stand-alone federated systems into smaller, more efficient platforms.
3. Ease of future technology refreshes to denser multicore silicon in similar processor families.

The key value of a hypervisor for aerospace and defense is separation of legacy hardware environments from new hardware environments, which significantly reduces both testing and upgrade time for all next-generation systems.

Chip Downing *is the Senior Director for Aerospace and Defense at Wind River. He can be contacted at chip.downing@windriver.com.*

Daily Briefing: News Snippets

By Sharon Hess, Assistant Managing Editor

www.mil-embedded.com/dailybriefing

Lockheed Martin/Navy contract eases mission planning

Mission planning is about to get a whole lot smoother, thanks to a $10 million contract between Lockheed Martin and the U.S. Navy. The contract stipulates that Lockheed Martin develops mission pre-planning software for crews of MH-60S and MH-60R multimission helicopters, enabling pilots to choose from different preconfigured mission plans that "tell" the aircraft's digital cockpit the route, communications frequencies, sensors, weapons, and navigation waypoints to implement once airborne (Figure 1). In addition to preconfigured mission selection, pilots can also integrate targeting and weather data, maps, and more using a planning-system laptop. The mission-planning information is then uploaded to the company's Common Cockpit avionics suite via a memory card to ease mission-planning intricacies. The new software is part of the U.S. military's COTS-based Joint Mission Planning System (JMPS), which will supersede legacy systems used for mission planning. Software deployment is slated for 2012.

Figure 1 | Mission planning will get a whole lot easier for MH-60R (pictured) and MH-60S multimission helicopter pilots, thanks to a $10 million U.S. Navy/Lockheed Martin contract for mission-planning software for the aircrafts' digital cockpit. Lockheed Martin photo

SM-3 missile program progresses

Making progress on the Standard Missile-3 (SM-3) Block IIA missile serves as impetus for a recent contract between the Missile Defense Agency and Raytheon Missile Systems Co. in Tucson, Arizona. The $165 million "cost-plus-award-fee with technical/schedule performance incentive contract" stipulates that Raytheon completes several preliminary design review tasks including design and development support, material for systems engineering, engineering services, and initial hardware fabrication for SM-3 Block IIA. SM-3 falls under the Missile Defense Agency's Ballistic Missile Defense System (BMDS) umbrella and is designed to thwart ballistic missile threats at a short to intermediate range. Meanwhile, Block IIA comprises a joint effort between the U.S. and Japan. Contract fulfillment is expected in March 2011.

Navy takes small steps to a weapons-class laser

In a move of incremental progress, the Office of Naval Research recently penned a $23 million task order relative to an existing cost-plus-fixed-fee/indefinite-delivery contract with The Boeing Company. The task order is "for the critical design of a 100-kW class Free Electron Laser (FEL) device." Falling under the nomenclature of Navy FEL Innovative Naval Prototype (INP), the 100 kW weapons-class FEL's development will render the engineering and physics data necessary to eventually develop an MW-class FEL. Work under the contract will occur in Albuquerque, New Mexico and Medford, New York, in addition to other subcontractor locales and government labs, with a completion date of December 2011.

DARPA surveillance goes nocturnal

Already having daytime surveillance technology in-hand, DARPA recently granted BAE Systems a $49.9 million contract to incarnate an advanced processor for the ARGUS-IR (Autonomous Real-time Ground Ubiquitous Surveillance – Infrared) nighttime IR system (Figure 2). BAE is responsible for two tasks under the nocturnal surveillance technology contract: 1) high-res IR sensor subsystem integration; and 2) design-through-test phases of ARGUS-IR's Airborne Processing Subsystem (APS). APS will store and process infrared sensor imagery, with a bit rate up to 200 Mbps and the capability to downlink at least 256 separate 640x480 video streams. Individual video windows can be specified as a "fixed video window" or as a "tracking video window." And finally, APS can automatically downlink image chips and metadata from moving targets. Designed for UAS compatibility, BAE's ARGUS-IR is slated for its maiden test flight by Q2 of 2012.

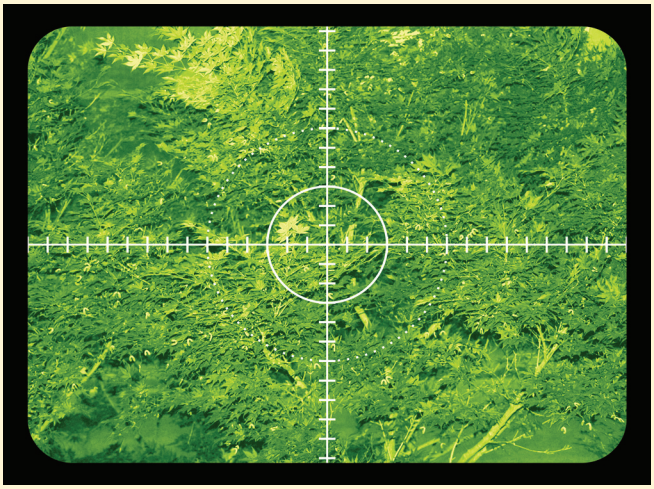


Figure 2 | DARPA recently contracted with BAE to incarnate an advanced processor for the ARGUS-IR nighttime infrared system, which might produce images similar to this one.

CompactPCI reports for duty

The U.S. military will once again see CompactPCI enlisted for duty, per a recent announcement that GE Intelligent Platforms has received from General Dynamics C4 Systems one of several anticipated orders with a cumulative expected value of $2.5 million, GE reports. The orders, to be implemented into the U.S. Army's Brigade Combat Team Modernization (BCTM) strategy, are for the NETernity 3U CompactPCI CP923RC-M Ethernet switches. Serving as the BCTM communications hub to be used by command and control systems, the switches will provide data exchange among various ground and unmanned air vehicles (Figure 3). The ruggedized, IPv6-supportive, fully managed, 10-port, layer 2/3 GbE switch is powered by OpenWare switch management software to ease network configuration woes and render addressing, switching control, monitoring, and routing capabilities. BCTM leverages Future Combat Systems (FCS) program-developed technologies and is geared to render improved protection, mobility, precision, and information via its blend of networked, mobile BCTs.

Figure 3 | A recent CompactPCI order is reportedly the first of several for BCTM's command and control systems' communications hub. U.S. Army photo

MoD's C2 gains interoperability and more

Interoperability is the name of the game these days for military technologies, obviously in hardware and apparently in software, per a recent contract between Northrop Grumman Corporation and the United Kingdom's Ministry of Defence (MoD). For an unrevealed monetary value, Northrop Grumman will provide an interoperability- and usability-enhanced version of its C2PC (Command and Control for the PC) command and control software for the MoD's JC2SP (Joint Command and Control Support Programme) to increase JC2SP's C4I capabilities. Beyond heightened interoperability and usability, C2PC enhancements comprise: more interfaces, Windows-capable clients, increased track database capability, and less required bandwidth during information transmission, in addition to more security. Meanwhile, JC2SP's mission is to deliver Network Enabled Capability (NEC) operational elements such as C2, decision, and planning tools by interconnecting C2 information and applications capabilities in the battlespace. JC2SP also provides integration and improved interoperability with the Defence Information Infrastructure (DII) program, slated to join 300,000 users and 150,000 terminals at 2,000-plus defense sites for deployed operations and shipboard.

For consideration in Daily Briefings, submit your press releases at http://submit.opensystemsmedia.com. Submission does not guarantee inclusion.

Figure 4 | A contract between Elbit Systems and Harris Corporation specifies that Harris renders engineering services for its Falcon tactical radio systems integration into Australia's Battle Management System.

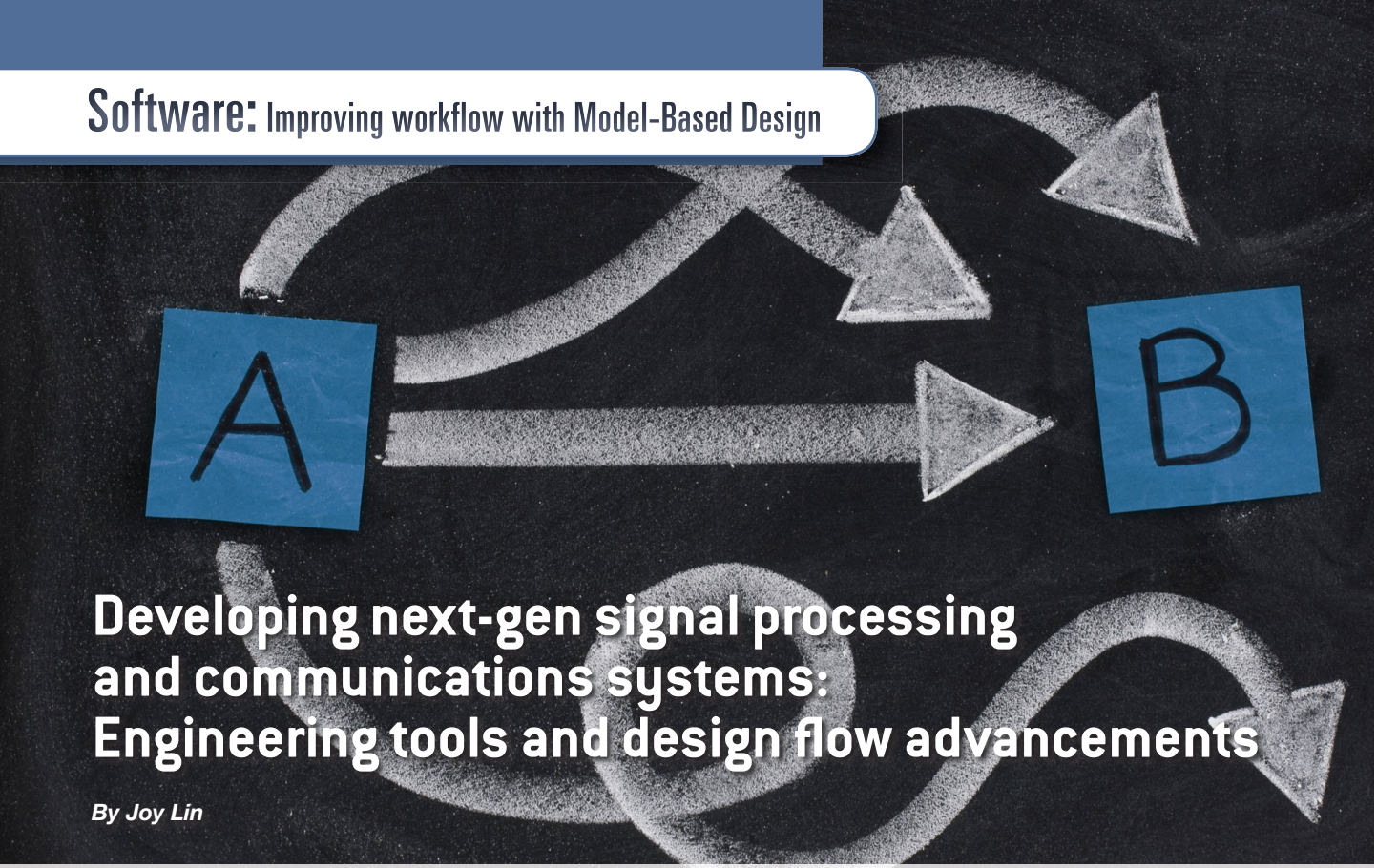
Secure interconnection is a universal need

Whether in the USA or a land far away … maintaining secure radio communications amongst military forces is imperative. The evidence: a recent three-year, $9.5 million contract supporting the Australian Defence Forces' (ADF's) communications modernization program dubbed "the Australia Department of Defence Land 200" (Figure 4). The contract between Elbit Systems and Harris Corporation stipulates that Harris renders engineering services for its Falcon tactical radio systems integration into the Battle Management System Elbit is building as contracted by the ADF. The lion's share of the contract calls for the Falcon III AN/PRC-152(C) radio, designed to satisfy U.S. JTRS requirements, to act as a hub for soldier-worn C4 technologies and connect the Battle Management System to soldiers to facilitate secure data and voice exchange.

Legacy Link 16 network terminals get (more) modern

Known for its information-sharing abilities relative to aircraft such as the F-15E Strike Eagle and F-18 Hornet, Link 16 tactical data link technology is about to get an update (Figure 5). Case in point: A recent $35 million cost-plus-award-fee/cost-plus-incentive-fee contract between the Space and Naval Warfare Systems Command (SPAWAR) and Data Link Solutions, LLC specifies that Data Link Solutions completes Link 16 network frequency remapping and crypto modernization modifications to SPAWAR's legacy Joint Tactical Information Distribution System (JTIDS) terminals. The contract's value could rise to $37 million and work completion could extend until March 2015, if stated contract options are exercised. If not, work completion is anticipated in November 2013.

Figure 5 | The Navy F-18 Hornet (pictured) and the F-15E Strike Eagle are examples of aircraft that could benefit from Data Link Solutions' forthcoming updates to SPAWAR's Link 16 network terminals. U.S. Air Force photo by Senior Airman Miranda Moorer



Developing next-gen signal processing and communications systems: Engineering tools and design flow advancements

By Joy Lin

It used to be that system engineers, algorithm developers, and hardware engineers used different tools to do their jobs, which often resulted in workflow gaps that led to design errors. However, with Model-Based Design (MBD), engineers use models as a golden reference that links every part of the development process – requirements, design, implementation, and testing. A traditional versus MBD workflow is examined, and multidomain modeling tool requirements definition, design trade-off study performance, in-model algorithm development, and verification against design requirements are also examined.

To accommodate tighter budget and time constraints for developing next-generation signal processing and communications technologies, continuity in design flow is becoming critical for engineers. Traditionally, system engineers, algorithm developers, and hardware engineers use different tools to do their jobs, which can introduce gaps in the workflow that may lead to errors in the design and delays in the development process. In contrast, by using Model-Based Design, engineers across disciplines use a common set of models in an extensible environment to define requirements, develop algorithms, implement or target hardware, and test and verify their designs.

Traditional workflow versus Model-Based Design

In a traditional workflow, requirements analysis and high-level design trade-offs are often done on paper or with a basic tool such as Excel or using expensive prototype hardware. Algorithm implementation in C or Hardware Description Language (HDL) is done manually, as are testing and verification. This process often requires several iterations between the algorithm design team and the C and HDL teams as a result of unclear requirements and design documentation or inherent design difficulties.

With Model-Based Design, system engineers use models to derive low-level requirements and then use the models to interface with customers and suppliers. They model the behavior of digital, analog, and RF components of the system and perform design trade-offs in simulation, which can be difficult or impossible using paper-based design reviews. Algorithm developers can then reuse and elaborate the same models to build and test more detailed designs. Further in the development process, these models can become the design artifacts from which hardware engineers automatically generate HDL code. Then the system-level models and tests can be reused as a test bench to validate performance of the HDL implementation and the final hardware against the model-level results.

With Model-Based Design, models are reused and elaborated at every development phase, reducing the amount of translation inefficiencies and errors in the process. With the model at the center of the design process, engineering teams also have a common platform to share the design (see Figure 1).

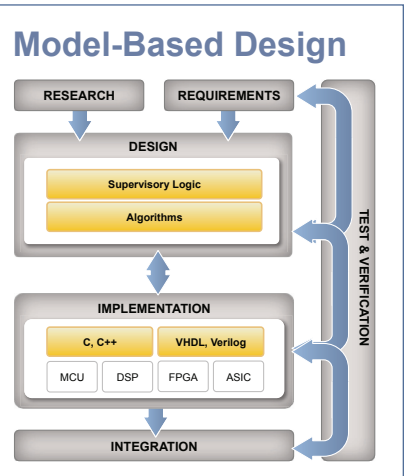


Figure 1 | Model-Based Design provides a multidomain tool environment and integrates all phases of development.

Defining requirements with a multidomain modeling tool

Modern signal processing and communications systems are characterized by complex and interconnected digital, analog,

mixed-signal, radar, and Radio Frequency (RF) subsystems. Further, at the beginning of a project, requirements are often incomplete or conflicting. Thus, the first step is to use the high-level requirements to derive well-defined, function-level requirements that can then be portioned into relevant subsystems. To illustrate using an example, the figure below is a set of high-level and functional-level requirements for an ISM Band FSK/GFSK/OOK/MSK/GMSK Transceiver[1]. The high-level requirements are: frequency bands of 862 MHz to 928 MHz, and 431 MHz to 464 MHz, with data rates of 1 kbps to 300 kbps. Digital function-level requirements are receiver sensitivity Bit Error Rate (BER) specifications (see Figure 2), and Intermediate Frequency (IF) receiver bandwidths.

To implement this set of requirements, the system engineer needs to break down the high-level functional block diagram into its digital and RF components. With Model-Based Design, the digital and RF components can be combined into a single model that allows the system engineer to make design trade-offs and analyze system performance to ensure that it meets the high-level requirements. Traditionally, optimal design trade-off comes from years of hands-on experience in the digital and RF domains, or from heritage design. Model-Based Design relies less on heritage knowledge and more on system-level simulation to find the optimal design.

The model can be used as a set of executable specifications and the model-level test vectors can be used as the acceptance criteria. Often, the process of creating the models and running simulations uncovers requirement errors at the beginning of a project, when they are less expensive and easier to fix compared to finding them in the implementation and testing stages, when fixes can be an order of magnitude more costly. The time and effort that engineers invest in creating the executable models at the requirement stage will pay significant dividends in the latter stages of the design process. Aerospace companies who use Model-Based Design typically reduce their verification time by about 90 percent primarily because bugs are typically discovered and removed in the design and simulation stage, instead of at the test stage.

FEATURES
Ultra low power, high-performance transceiver IC
Frequency bands:
– 862 MHz to 928 MHz – 431 MHz to 464 MHz
Data rates supported:
– 1 kbps to 300 kbps
1.8 V to 3.6 V power supply Single-ended and differential PAs Low IF receiver with programmable IF bandwidths:
– 100 KHz, 150 KHz, 200 KHz, 300 KHz
Receiver sensitivity (BER):
– 116 dBm at 1.0 kbps, 2FSK, GFSK – 107.5 dBm at 38.4 kbps, 2FSK, GFSK – 102.5 dBm at 150 kbps, GFSK, GMSK – 100 dBm at 300 kbps, GFSK, GMSK – 104 dBm at 19.2 kbps, OOK

Figure 2 | Sample high-level and function-level specification of a High Performance, Low Power, ISM Band FSK/GFSK/OOK/MSK/GMSK Transceiver IC[1] illustrates the type of high-level requirements that system engineers receive.

Performing design trade-off studies

As mentioned, by using a multidomain Model-Based Design environment, engineers can perform simulations early in development and make effective trade-offs in designs. For example, to study how best to meet the system-level BER requirements, systems engineers can explore design options by swapping in different types of IF receiver architectures and modulation and demodulation schemes in a single tool environment.

Simulating the models can also eliminate guesswork. Instead of relying on heritage design to understand what would be adequate margins in each phase, effective frequency margins can be lowered because gains and losses at each stage can be better understood via simulation than static analysis.

Developing algorithms in models

The system-level models used for requirement definition can be reused, thereby serving as a basis from which a detailed algorithm design can be developed. Modeling tools generally provide libraries of common building blocks, such as common filters and amplifiers. Teams can also develop and share custom building blocks, reducing the amount of duplicate effort across projects or companies.

In the past, engineers had to use a system-level tool to create an overall system model representation that was different and disconnected from tools that allowed for detailed modeling and exploration of the algorithms within the system. Recent advancements in algorithm modeling tools help engineers build and maintain a single integrated model that captures the overall system complexity and the interaction of

various subsystems. For example, tools now support stream processing for continuous acquisition of live data, processing large signal and image data files, and for embedded implementation, while maintaining tight integration with system-level modeling tools. In addition, these tools support automatic management of state information, data indexing, and buffering, which are particularly useful for iterative or stream-processing algorithms.

Verifying implementation against design requirements

A key benefit of building models and running simulations of executable system specifications is that those models can then help engineers significantly improve the efficiency and the quality of results of the final system implementation.

As a modern signal processing or communications system design moves through the design flow, an early key elaboration stage is identification of the portions of the design suitable for implementation on a fixed-point DSP, a microcontroller, an FPGA, or an ASIC. To make this assessment, engineers must convert the early floating-point designs to fixed point. However, fixed-point conversion is one of the major challenges in communication systems workflow. Traditionally, at this stage, engineers would take the floating-point system models as a starting point and recode major portions of the design in fixed-point C or HDL, resulting in delays, bugs or flaws, and wastage of time and resources. Rather than writing or rewriting the algorithm in C and manually converting it to fixed point, Model-Based Design tools often provide automatic fixed-point conversion capabilities. In many cases, engineers can now build and maintain a single polymorphic reference model that can be run in floating-point or fixed-point as needed. In Model-Based Design, the models that were used to design algorithms can be used to automatically generate C or HDL. By connecting the algorithm design environment to the code implementation environment, engineers reduce the number of errors introduced during translation.

Verification can be completed through co-simulation of the system-level models with the final C or HDL design. At this stage, the system-level models are reused as the test bench. Through this reuse, engineers save time writing test bench code and creating test vectors. This close coupling between design, implementation, and verification not only saves time when compared to coding manually, but also helps minimize implementation errors.

Reference:

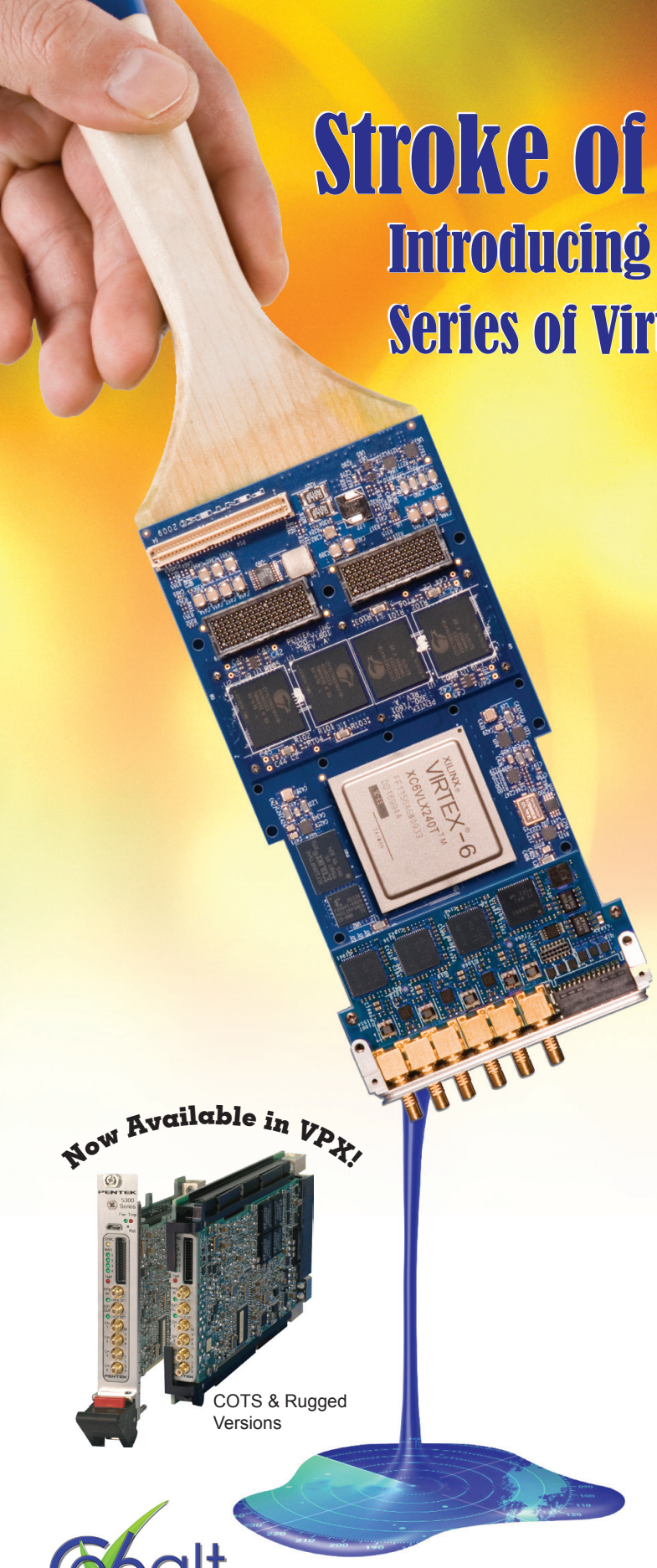
[1] Analog Devices, Technical Data ADF7023 – High Performance, Low Power, ISM Band FSK/GFSK/OOK/MSK/GMSK Transceiver IC www.analog.com/en/rfif-components/rfif-transceivers/adf7023/products/product.html

Joy Lin *joined MathWorks in 2008 as Aerospace and Defense Industry Marketing Manager. Prior to this, she worked at Boeing Defense, Space & Security in El Segundo, California. She holds a bachelor's degree in Aerospace Engineering from the Massachusetts Institute of Technology and an MBA from the MIT Sloan School of Management. Joy can be contacted at Joy.Lin@MathWorks.com.*

MathWorks
508-647-7159
www.MathWorks.com

Stroke of Genius

Introducing the NEW Cobalt Series of Virtex-6 Modules!



Unleash your inner genius with Pentek's new 71620 Cobalt™ Virtex-6 XMC module. Built to optimize high-performance, wideband, communications, SIGINT, radar, beamforming and telemetry applications, this high-speed module includes:

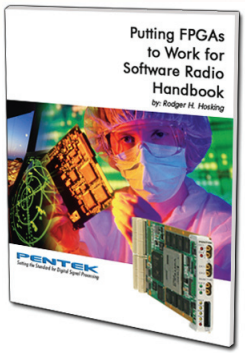
- Three 200 MHz 16-bit A/Ds
- Dual 800 MHz 16-bit D/As
- Intelligent chaining DMA engines
- High dynamic range
- PCI Express x8
- Dedicated memory for each I/O stream
- Secondary x8 XMC for gigabit serial I/O
- Advanced gating and triggering modes optimized for radar applications
- Multi-channel, multi-board synchronization
- GateFlow® FPGA Design Kit
- VPX, XMC, PCI, PCIe, VME/VXS, cPCI, conduction-cooled XMC

With extensive resources and new enhancements in DSP engines, block RAM, logic and clocking technology, the Virtex-6 family represents the industry's most advanced FPGAs.

Now Available in VPX!

COTS & Rugged Versions

Call 201-818-5900 or go to www.pentek.com/go/mescobalt for your FREE *Putting FPGAs to Work in Software Radio Handbook*, technical datasheets and price quotations.



Cobalt

PENTEK
Setting the Standard for Digital Signal Processing

Pentek, Inc., One Park Way, Upper Saddle River, NJ 07458 Phone: 201.818.5900 Fax: 201.818.5904 e-mail:info@pentek.com www.pentek.com

U.S. Navy photo by Mass Communication Specialist 3rd Class Adam K. Thomas

"Smart" COTS multifunction I/O designs revolutionize data distribution systems

By Paul Feldman

As modern and future platforms increasingly rely on electronics for control, weapons management, and sensor data integration, the number of sensors and control points used in these platforms has expanded exponentially. Coinciding with this expansion is a significant increase in the requirements for handling this sensor data, while real-estate savings needs and redundancy requirements increase. However, "smart" distributed I/O boards and Sensor Interface Units (SIUs), when implemented prudently, can satisfy the demands of these conflicting requirements.

Modern military platforms increasingly rely on electronics for operation. Just as aircraft have transitioned to fly-by-wire systems, ground vehicles are transitioning to drive-by-wire. Simultaneously, greater numbers of sensors are being incorporated into sea, air, and ground vehicles, and these sensors are used to detect everything from incoming projectiles to engine vibration. Coinciding with this are increasing numbers of electronically controlled actuators to affect a response based on the sensor data. Each of these sensors and actuators must be connected to some type of I/O point to collect data for processing. As an example, consider a simple turn-by-wire design. The operator (driver) turns right, requiring an input measurement. Then a control point is used to activate the correct actuator to change wheel position around the vertical axis.

So the question is: How do we manage the increased electronic content of all these sensors without increasing size or weight, then process this exponential increase in data? As always, using more electronics implies higher processing requirements and an increased number of interconnects, which raises even more issues. The answer to this paradox lies in modern "smart" distributed I/O boards and Sensor Interface Units (SIUs), which can satisfy the need for:

- High levels of analog integration
- Sophisticated processing within modern bandwidth limits
- Meeting tightening real-estate requirements
- Easing I/O data and processing distribution
- Mission-critical redundancy

High analog integration levels: "Smart" I/O helps

To accommodate this sensor-induced, increased demand on electronics, using high levels of analog integration proves a viable remedy: two to three times the number of I/O points can be placed on a single PCB today than in the recent past. "Smart" I/O boards help increase analog density by performing many functions previously performed by ancillary analog circuits digitally, such as calibration, filtering, and BIT. Although certainly not proceeding at the same pace as digital electronics integration, nonetheless, analog integration is proceeding along a rapid slope. Whereas five years ago, 32 A/Ds or D/As on a single PCB was considered high density, today 60 or more is commonplace. In fact, it is now to the point that the number of analog functions that can be placed on a PCB is limited more by the number of I/O pins on the connectors than by the density of the electronics that can fit in a given PCB real estate. To address this problem, manufacturers are turning from VME or CompactPCI to VPX (VITA 46). VPX has approximately twice the I/O of VME.

"Smart" I/O boards: Sophisticated processing

The I/O boards being provided today are "smart." These boards not only perform A/D, D/A, or simple I/O functions, but they also provide sophisticated data-processing levels. For example, simple I/O boards have A/D converters that sample the input data at rates from thousands to millions of samples per second, then send that data to a mission computer for processing. Modern military ships, submarines, aircraft, and even ground vehicles can have many thousands of points to sample. For example, think of the thousands of vibration sensors needed on a modern submarine to ensure complete stealth.

Additionally, in the desire to gain more information over ever-rising bandwidths, the sampling rate is increasing from a few thousand Hz to more than 100 KHz, with bit depths increasing from 12 bits to 16 and 24. These data rates can easily overwhelm the most powerful processor, especially when complex algorithms like FFTs and FIR filtering need to be performed. With onboard FPGAs and DSPs, I/O board manufacturers can easily provide preprocessing to offload the main processor. Since these components are highly programmable, the hardware of these COTS boards remains the same. However, the functions provided are highly configurable.

Meeting shrinking real-estate requirements

"Smart" I/O boards provide yet another important feature that minimizes system size and power: the ability to perform

multiple functions on one PCB. In the past, many boards were available with 32 or 64 A/Ds or D/As or 28 V discretes, as well as separate boards for different types of communication functions (MIL-STD-1553, serial, ARINC 429, CANbus, and so on) and processing (SBCs). Many systems today, however, require smaller numbers of different types of I/O and communications.

To address this, manufacturers have created multifunction VME, CompactPCI, and VPX boards. These boards allow the system integrator to select from a large number of available functions and to incorporate smaller channel counts of many functions on one PCB. This is made possible through the baseboard FPGAs' and DSPs' ability to be programmed at final assembly to perform almost any task. For example, a single board can incorporate A/D, D/A, RTD, MIL-STD-1553, and ARINC 429, just to name a few.

Another possibility for real-estate savings is to use a multifunction I/O board that contains PowerPC- or Intel-based SBC support and the ability to provide large combinations of functions. A single board can replace up to six dedicated boards. Just as importantly, multifunction boards such as these can be COTS-based.

I/O data distribution and processing

The concept of I/O data distribution and processing is extremely powerful and can simultaneously solve a host of issues, such as reducing cable weight and mission computer processing requirements. The Sensor Interface Unit (SIU), shown in Figure 1, is usually some type of rugged, self-contained design that includes configurable I/O and provides communications with a mission processor. This approach allows system integrators to place I/O points very near the actual sensors, preprocess the data, and then send the reduced data back to the mission computer.

Figure 1 | NAI's Sensor Interface Unit

A small number of cables (usually just wire or fiber GbE) now needs to run from the SIU back to the main processor. One or more remote SIUs containing all of the I/O functions needed to perform this task, as well as an SBC function, could be used. The SIUs could be placed within a few feet (versus hundreds or even thousands of feet for systems with a single chassis) of the sensors and actuators to implement the control processing necessary to perform the actual function.

This situation presents significant weight reduction advantages: The weight difference between 100 twisted/shielded pairs, 50 feet in length versus a dual GbE wire or fiber connection of the same length is enormous – greater than a 10 to 1 reduction. Shorter cable lengths also result in reduced noise pickup, wire losses, and ground loop potentials, and in many cases reduced EMI. This can be most advantageous in aircraft, where hundreds of wires now need to travel only a few feet, versus 100 feet or more, or on ships and submarines that can be many hundreds of feet in length. Since such an SIU might use standard 28 VDC or single/three-phase 115 VAC, for example, the power cabling to the SIU is also short because this standard power is usually available across the entire platform at many points.

Redundancy is a good thing

Redundancy is another area where the SIU approach excels. Previously, redundant systems required entire racks of equipment to be duplicated, with the issue of which hardware and software decide which rack is in control, along with which processor. Usually, if anything failed in one rack, the entire rack needed to be shut down, and the backup took over. Distributed SIUs, however, can provide an inherent "fail-soft" property. Since each SIU controls a subset of all platform functions, if an SIU fails, only that subset needs to be switched over to the backup hardware. Additionally, each SIU likely has multiple GbE or other communications channels, so each is always connected to both the main and redundant mission computers. The main mission computer can stay in control of the system, despite various hardware failures. Figure 2 shows a conceptual redundant system design using this approach.

One manufacturer, North Atlantic Industries, offers an SIU that supports up to 300 I/O points – configurable for many different I/O functions – providing the equivalent of an SBC to process data and communicating to the main mission processor over a multitude of communication interfaces including GbE, MIL-STD-1553, ARINC 429, and CANbus, just to name a few.

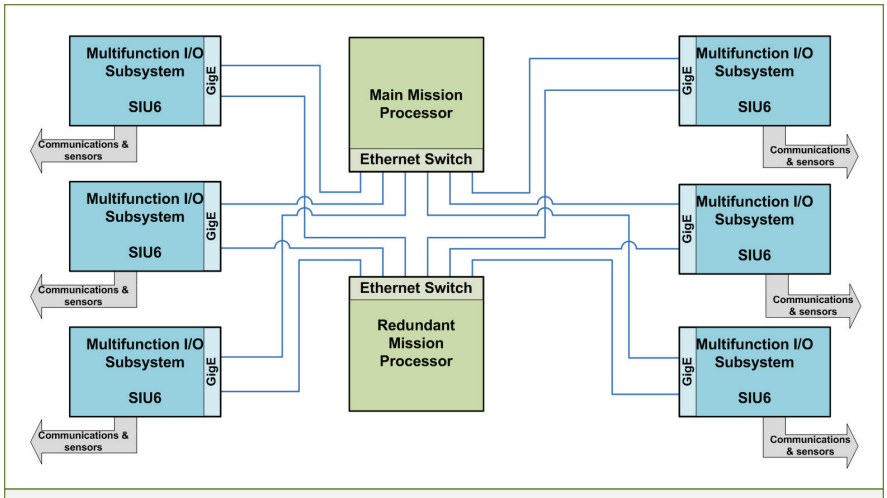


Figure 2 | "FailSoft" system using SIUs and redundant mission processors

Paul Feldman *is V.P. of Digital Design Engineering at North Atlantic Industries. He has more than 30 years of experience in system, software, and electronic design. He received his BSEE and MSEE from the Polytechnic Institute of New York. He can be contacted at pfeldman@naii.com.*

North Atlantic Industries
631-567-1100 • www.naii.com

U.S. Air Force photo by Tech. Sgt. Efren Lopez

Enhanced Full-Motion Video advances military UAS surveillance:

Multistream image processing and routing in real time

By Jack Wade

Live Full-Motion Video (FMV) from UASs has become indispensable in military and intelligence operations. As these video streams play an increasing role in warfighting, inconsistent or poor image quality is becoming a threat to mission success. Fortunately, advances in FPGA-based parallel processing technology now allow real-time image processing that can significantly improve the quality and usefulness of UAS video feeds. An FMV-routing platform is also integral in ensuring FMV data gets into the right hands.

Military strategists are tooling up with Unmanned Aircraft Systems (UASs) to provide the visual surveillance today's combat environment requires. Last year, for the first time, the Air Force trained more unmanned aircraft pilots than conventional fighter and bomber pilots combined. Robotics, and particularly UASs, have changed the nature of warfighting.

UASs can transmit a direct video feed to a nearby ground control station or broadcast via satellite to command centers around the globe. They provide an on-demand, close-up view of the combat zone that would not otherwise be possible. UASs make it possible for commanders to make decisions and execute missions from a safe distance without endangering the lives of their troops. The key enabling technology responsible for the breakthrough capabilities of the UAS and the subsequent transformation of warfare is Full-Motion Video (FMV). Practically speaking, without FMV from the aircraft's onboard cameras, pilots would not be able to navigate the UAS remotely from the ground (Figure 1).

The problem is that even the most sophisticated camera, from the best vantage point, may not be able to provide the clear and reliable visibility needed for mission-critical applications. For example, field deployed UAS aircraft encounter atmospheric conditions such as dusk, dawn, fog, haze, smoke, and bright sunlight. Furthermore, producing high-quality imagery on a mobile platform such as the UAS poses some interesting challenges due to its motion and the resulting image perspectives. The quality of the video imagery can be compromised by narrow camera field-of-view, data link degradations, bandwidth limitations, or a highly cluttered visual scene as in urban areas or mountainous terrain. In fact, the military reports that inconsistent quality of FMV imagery is a serious problem. Mission success often depends on the ability to positively identify targets, and this requires clear – and in many cases, enhanced – imagery.

Fortunately, it is now possible to address these problems and to significantly enhance FMV image quality. Recent advances in FPGA-based parallel processing

Figure 1 | Practically speaking, without FMV from the aircraft's onboard cameras, pilots would not be able to navigate the UAS remotely from the ground. U.S. Air Force photo by Senior Airman Tiffany Trojca

technology now provide the computing power necessary to use sophisticated image processing software algorithms that can yield dramatically enhanced FMV in real time. A platform for routing FMV into the proper hands is also integral.

Parallel processing breaks the speed barrier

The science of digital image processing has resulted in a large body of useful software algorithms for image processing. Most of these algorithms were originally developed to process still images. These algorithms tend to be computationally intensive, and in the past, processor technology did not offer the speed necessary to keep up with the demands of FMV. To understand the processing requirements for FMV, consider the following example. The number of frames per second, the number of lines per frame, and the number of pixels per line depend on the video standard. The National Television System Committee (NTSC) standard definition video is digitized at 720 x 480 or full D1 resolution at 30 frames per second, which results in a 10.4 MHz pixel rate. Furthermore, High-Definition (HD) video standards have up to six times more data per frame. The computation load, therefore, can be six times higher.

The actual amount of processing required per pixel depends on the image processing algorithm. For example, a popular edge detection algorithm requires approximately 130 operations per pixel. Coupled with running at multiple resolutions, serial implementation of the algorithm using a programmable DSP with a clock speed of 600 MHz can only process 4.6 mega pixels per second. This is not sufficient to support real-time video streams at high resolution. High-Definition Full-Motion Video (HD FMV) streaming, for example, is more suited to processing algorithms at 30 fps at full resolution of 1,920 x 1,080 pixels: a pixel rate of 160 mega pixels per second. Additionally, the time required to process one sample can be longer than the time between the arrivals of two consecutive samples, such that the operations need to be executed in parallel. Consequently, real-time processing of digital video signals requires parallel processing to handle the high data throughput.

Today, there are FGPAs that can process FMV – and be scaled to handle any number of video streams – in real time. The advantage of FPGAs compared to other processors is their unmatched capacity for parallel processing. FPGAs benefit from an arbitrary number of data paths and operations, up to the limit of the device capacity. But as fast as FPGAs are, achieving the goal of zero latency required for real-time FMV requires some ingenuity. The trick is to calculate the necessary adjustment based on the first frame, but apply it to the following frame, and so on. Calculations for the next frame are done in parallel with processing of the current frame, so no latency is introduced.

Open-architecture algorithms afford quality imagery

Using an image processing platform based on FPGAs makes it possible to apply existing and new image processing algorithms to address the many obstacles to high-quality FMV imagery.

Such a platform would benefit from an open architecture that would facilitate algorithm porting and thus make it easier to tap into a wide variety of image processing algorithms that are commercially available.

Existing image processing algorithms offer countless possibilities for deriving new useful information from FMV streams.

There are image enhancement algorithms that filter out visual distractions while adjusting contrast and color to aid the eye in focusing on elements of interest. Other algorithms can pinpoint a subject hidden within a large landscape, like finding a needle in a haystack. Image mosaic algorithms can stitch together images from multiple cameras and multiple view angles to form a single unified higher-resolution view. There are also encoding/decoding and compress/decompress algorithms that make image data transmission and storage more efficient. Algorithms can be used individually, or multiple algorithms can be applied to the same video stream.

Image processing algorithms that are FPGA-based can operate in both parallel and sequential modes. In a parallel mode, an image frame can be simultaneously fed into multiple FPGAs, each working on its assigned area of interest. In a sequential (or daisy-chaining mode), the output of one FPGA is fed into a subsequent FPGA for additional processing. For example, a video stream might first need processing to eliminate spatial or temporal noise, before it flows into a second algorithm where stabilization, object recognition, or other functions occur. Thus, many different types of algorithms are important for UAS applications (Figure 2). These algorithms include chroma keying, stabilization, fusion, locally adaptive contrast, and tracking movers, among many others.

A platform for dynamic, enhanced FMV routing

Capturing quality imagery at real-time speeds is only part of the solution. It is equally important to be able to route the right visual information to the right person at the right time. For example, ground station personnel may use FMV from a UAS to pilot the aircraft, while command personnel in Washington will require different views of the same video feed to identify targets.

An integrated platform combining large-scale video routing capabilities with sophisticated image processing would be ideal for military field operations. This platform might use a switched fabric to serve as a video matrix switch to allow any video input to be routed to any video output, including multiple outputs. Video inputs could be routed to any of the algorithms, or any combination of algorithms. Such a platform could take any video source and route it to any combination of attached displays or network connections. It could route multiple sources to one monitor, or to virtual screens within a monitor. Operators could turn image processing functions on or off, or swap the primary and picture-in-picture windows using a touch screen.

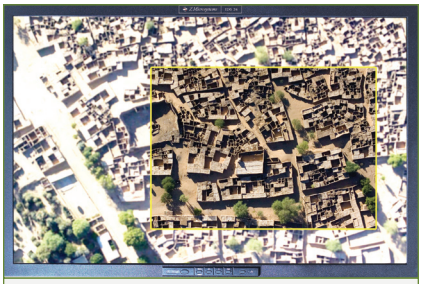


Figure 2 | Many different types of algorithms are important for UAS applications. On this display, an algorithm dehazes images for fog, smoke, and sand-storm environments.

This type of platform provides mission-configurable chat, moving maps, heads-up display, sensor video, and situational awareness. For UAS surveillance, this technology could be installed at a UAS Ground Control Station (GCS) to apply image enhancement and edge detection algorithms to incoming video streams. The edge detection algorithm would identify anomalous shapes and highlight details for surveillance and Bomb Damage Assessment (BDA).

Groundbreaking image clarity

Live, high-quality, real-time FMV from UASs has become indispensable in military and intelligence operations. New COTS systems that take advantage of FPGAs for real-time, scalable image processing – such as the Z Microsystems Any-Image-Anywhere (AIA) system – provide visual clarity not possible before.

Jack Wade *is Founder and CEO of Z Microsystems, a manufacturer of rugged, mission-ready computers and display equipment for the U.S. military. He is a recognized integrator and signal-processing expert. He regularly works with the USAF and UAS suppliers to enhance UAS performance. He can be contacted at jack.wade@zmicro.com.*

Z Microsystems
858-831-7010
www.zmicro.com

Understanding ARINC 661 and its benefits in a certified environment

By Yannick Lefebvre

The ARINC 661 avionics display standard has been in existence and evolving for close to a decade – with its most recent iteration published earlier this year. Yannick examines the ARINC 661 architecture, its Cockpit Display System (CDS) and User Application (UA) components, the standard's widget library – and how they all relate to DO-178B certification.

The task of creating aircraft cockpit displays has grown increasingly difficult over the past decade due to certifications rules (DO-178B) being applied more widely on military programs – along with the constant drive to deliver on shorter deadlines. To make things even more complicated, many players in the industry use their own development methodologies with little to no guidelines on content other than the instructions of their developers and human factors engineers.

This lack of a standards-based approach led to the proliferation of monolithic applications, either developed internally or through the use of commercial tools. These applications always need to be recertified as a whole, no matter which type of change is made. Exchanging data between commercial tools is also usually difficult, making it a challenge for aircraft manufacturers to think about switching providers for a system during the life cycle of an aircraft – or to reuse display elements between projects that are built using different software architectures.

In the late '90s, a committee of representatives from the industry was formed to address these concerns and put together a standard and flexible architecture for the creation of aircraft avionics which became ARINC Specification 661: Cockpit Display System Interfaces to User Systems. Today, ARINC 661 is used on programs such as the Airbus A380 and A400M, the Boeing 787 and the AgustaWestland Merlin Helicopter Upgrade. This standard has been used in the military realm since its inception, with its most recent iteration published earlier this year.

After learning about the ARINC 661 standard and its architecture, we'll look at the Cockpit Display System (CDS), User Application (UA), and widgets of ARINC 661, along with the benefits they bring to the table – especially for projects that need to be certified.

ARINC 661 architecture overview

While cockpit display software has traditionally been written as self-contained executables that present information and render graphics based on internal data, rules, and logic, ARINC 661 introduces a clear separation between the code drawing the graphics and the code managing the logic and the position and state of all visual elements. These two components are the CDS and the UA.

Furthermore, ARINC 661 defines the CDS as a runtime interpreter capable of displaying one or more elements from a finite library of building blocks called *widgets* based on information contained in external layout files. Finally, ARINC 661 defines a standard communication protocol for the CDS and UA to exchange messages. Figure 1 shows the relation between the CDS and UA, along with their typical execution environments and the communications between these two applications. It also shows that more than one UA can communicate with a CDS. In that situation, each UA can be developed separately and is responsible for updating and reacting to events of a specific section of the display.

A direct benefit of this architecture is that updates to the display composition are

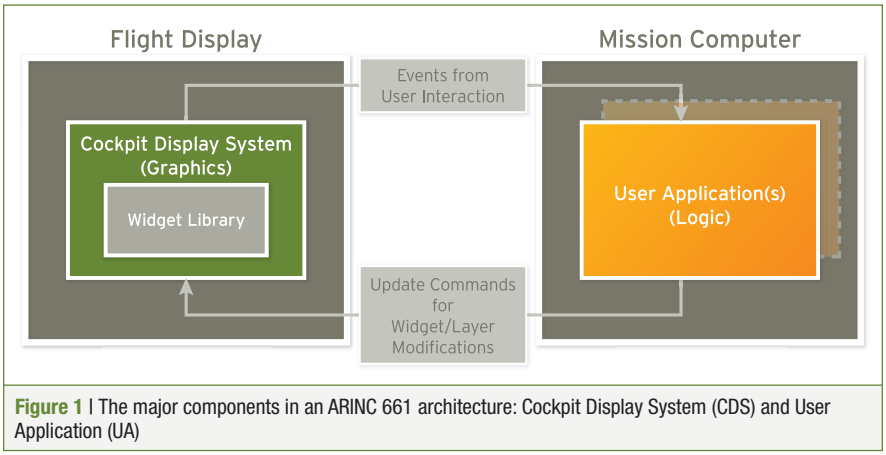


Figure 1 | The major components in an ARINC 661 architecture: Cockpit Display System (CDS) and User Application (UA)

done by creating new layout files instead of modifying code within a unified application. In a certified environment, this means that UA and CDS code does not need to be recompiled or recertified for visual layout changes such as repositioning or changing the visual attributes of display elements. The same benefit applies to changes to the logic flow of the application, which will only result in changes to a specific user application, leaving the CDS code base and other user applications unaffected.

Beyond isolation benefits, this approach also simplifies the distribution of application development between different teams within an organization or across subcontractors.

A closer look: CDS and UA

Looking closer at a typical ARINC 661 application execution flow, the CDS loads and displays widgets based on one or more layout files called *Definition Files* (DFs). Each DF contains one or more layers, which are hierarchical listings of all widgets that need to be loaded along with their initial parameters such as position, size, and visibility. They are natively stored in a binary format that is loaded into the CDS application at runtime.

> "A direct benefit of this architecture is that updates to the display composition are done by creating new layout files instead of modifying code within a unified application."

The standard also defines an XML interchange format to facilitate DF inspection, revision control, and sharing.

Going down a level, the physical display attached to the CDS is divided into one or more subsections, simply called *windows,* which can each render one or more layers. These windows cannot have any overlaps and will stack the designated layers to create the final result that will be shown to the pilot or operator on-screen. Figure 2 illustrates this hierarchy.

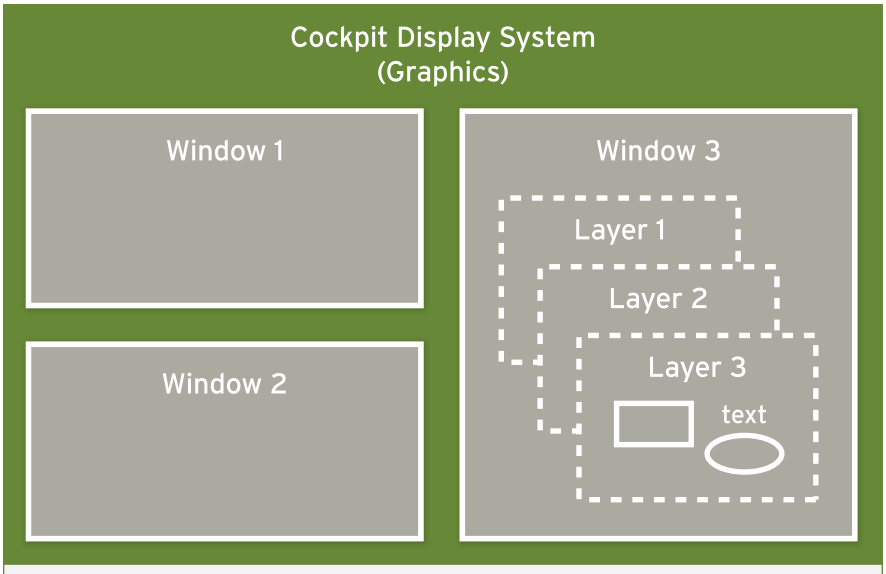


Figure 2 | CDS visual hierarchy

At runtime, the CDS handles pilot inputs and determines if these interactions can be handled locally (for example, the CheckButton needs to be highlighted when the cursor is placed over the widget) and/or if they should be transmitted to a UA (for example, that the CheckButton is pressed). In the latter case, an event is sent to the appropriate UA to determine a response based on the current system state and the event type. The UA(s) will also typically be sending a steady stream of messages to the CDS to update the position of all screen elements that are presenting information to the pilot.

When it comes to certification, this detailed display architecture greatly simplifies the creation of high- and low-level requirements. The use of a standard XML interchange format for Definition Files also gives flexibility for content developers to use CDS systems from multiple vendors as they see fit since

work can be loaded in any ARINC 661 compliant CDS. It is also possible to reuse large parts of a Definition File and a system's User Application(s) on a new project by only changing the visual appearance of widgets within the CDS library.

Standard widget library

Instead of being bound to a specific tool's application-building components, or creating a custom component architecture internally for a project, the ARINC 661 Specification introduced 42 widgets that could be used to create displays. This number went up to 50 with the first update to the standard, to 57 with supplement 2, to 65 in revision 3 and to 68 with its most recent incarnation published earlier this year.

Widgets vary in complexity from basic graphical elements such as the GpLine and GpRectangle widgets to complex objects such as the MapHorz widget, which displays maps from various data sources. There are also some widgets that do not have any visual representation that are used to group other elements together as well as apply transformations on them. An example in this last category is the MutuallyExclusiveContainer widget that groups multiple elements under a single parent but only displays one of its immediate children at a time.

While ARINC 661 describes how widgets should function and what their parameters are, it does not define their visual appearance. This gives full liberty to the display manufacturers to implement their own look and feel for a given project. There is also a provision in the standard to allow developers to create custom widgets with tailored functionality and parameters that still follow general widget creation patterns.

Having a standard set of widgets to develop a display makes it easy for a developer to become familiar with the ARINC 661 standard and to understand quickly how to develop new displays. Also, similar to the overall ARINC 661 architecture tying directly into high-level requirements, having a standard set of widgets with well-documented functionality helps accelerate the documentation of low-level detailed functional requirements for a certified project.

The future of ARINC 661

While the implementation of this architecture might seem a bit daunting – considering the need to put in place a compliant CDS runtime software architecture, a functional widget library that adheres to the specification, and tools to facilitate the creation of Definition Files and their output to standard binary files – it should be noted that COTS tools are available to provide these capabilities out of the box. In some cases, these tools are even qualified development tools that can generate qualifiable code under DO-178B. After seeing a few large commercial aircrafts lead the way, many programs, both commercial and military, are considering or have already adopted ARINC 661 for their upcoming projects, ensuring the success of this standard.

Yannick Lefebvre *is a senior application developer at Presagis. With a background in computer sciences and 13 years of experience in modeling and simulation, Yannick has provided counsel on hundreds of simulation and embedded display programs globally and is considered an expert in the industry. He can be reached at yannick.lefebvre@presagis.com.*

Presagis
514-341-3874
www.presagis.com

U.S. Air Force photo by Tech. Sgt. Paul Dean

Using a rapidly evolving ecosystem to develop optimized OpenVPX systems

By Thomas Roberts

OpenVPX (VITA 65) design principles and a rapidly maturing component ecosystem support development of next-generation embedded computing systems.

The pressure is on defense programs to deliver advanced next-generation capabilities and to deliver them fast. This includes programs for military communications, missile defense, and, most especially, ISR programs. In the words of Defense Secretary Robert Gates, "Our conventional modernization programs seek a 99% solution in years. The wars we are in require 75% solutions in months[1]."

Secretary Gates is pushing hard for faster program deployments because of the advantages new technologies can bring to our warfighters. For example, an advanced electro-optic camera mounted in a UAV can provide finely detailed images of areas occupied by insurgent forces. If those images could be combined with data from a SIGINT system, the result would be a rich picture of what is happening and where it is happening. New ISR programs are being designed to deliver this type of valuable information to warfighters by combining – in real time – data from different types of sensors.

Powerful, flexible, configurable embedded computing is essential to delivering these next-generation capabilities. The new sensors, including electro-optic cameras, SIGINT antennae, and sophisticated radars, are generating huge volumes of data that must be processed in real time. Then even more processing is needed to execute the complex algorithms that synchronize and combine output from multiple sensors. The computing subsystems must deliver powerful, real-time processing and also support flexible configurations that can deal with different types of processing and many I/O protocols.

Meeting these challenges requires an embedded computing architecture supported by a wide range of processing, I/O, and storage options. In industry terms, this means a robust ecosystem with a great number of compatible choices. Meeting the computing challenges and satisfying compressed delivery schedules requires that the components of this ecosystem can be selected, designed into a functional subsystem, integrated, tested, debugged, and finally deployed in a predictable fashion, without undue risk. The OpenVPX (VITA 65) standard meets these requirements, defining an embedded computing architecture supported by a robust and growing ecosystem.

The OpenVPX ecosystem matures quickly

In 2009 and 2010 the OpenVPX standard made huge strides in both system-level maturity and in the breadth of its ecosystem. First, the OpenVPX Industry Working Group, an alliance of VITA member defense and aerospace prime contractors and embedded computing systems suppliers, came together to address VPX (VITA 46) system-level interoperability issues. Many of the original VPX subspecifications, known as "dot specifications," had been developed without a top-down system-level approach supporting multivendor interoperability (Figure 1). As a result, the initial attempts at VPX implementations using components from multiple vendors were difficult to integrate, interoperate, and specify at the systems level. OpenVPX addressed this issue.

The OpenVPX specification developed by the Working Group was released to the VITA 65 working group within VITA and in June 2010 the OpenVPX System Specification was ratified as ANSI/VITA 65.0-2010 describing OpenVPX as "… the architecture framework that defines system-level VPX interoperability for multivendor, multimodule, integrated system environments."

OpenVPX uses the concepts of planes, pipes, and profiles to provide a standards-based basis for interoperability. It defines multiple planes for Utility, Management, Control, Data, and Expansion, as well as various sizes of pipes used for serial communication. There are also several types of profiles for structure and hierarchy in the specification (slot profile, backplane profile, module profile, and development chassis profile). The backplane profiles define the backplane topology (types: centralized and distributed switching, and host/slave).

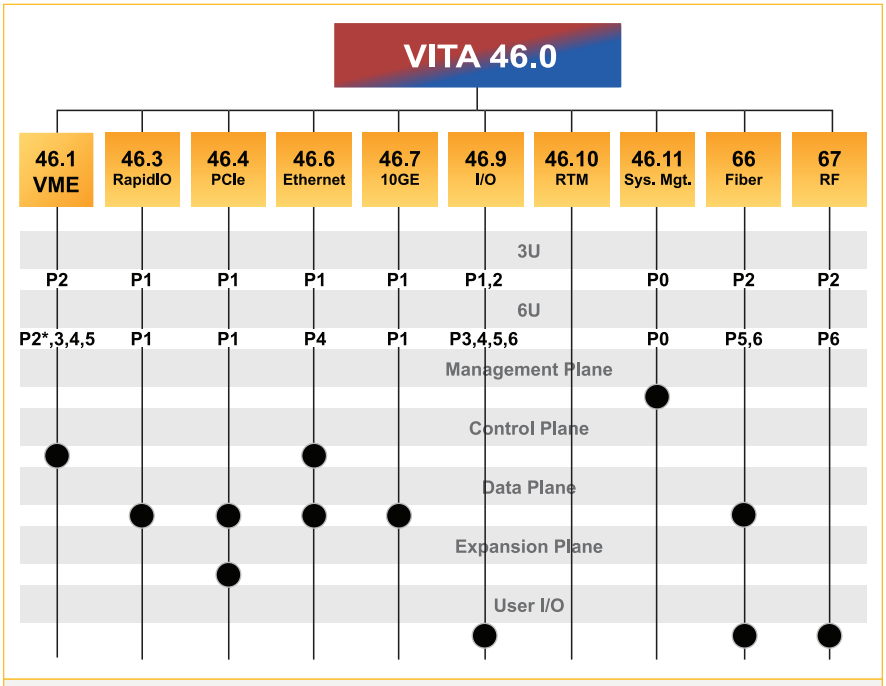


Figure 1 | VITA 46.0 and VITA 46.x dot-specification matrix

By expanding VPX with OpenVPX, the industry came together in a focus on system-level interoperability. Well before final ratification, the technology vendors that participated in creating OpenVPX, as well as many other companies, began to design, develop, and deliver products that adhered to the OpenVPX standard, rapidly creating a continually growing ecosystem. Just a partial list includes:

- BittWare Signal Processing Systems – FPGA and DSP processing modules
- Concurrent Technologies – Intel processing and storage modules, and XMC carrier card
- Elma Bustronic – Backplanes/Chassis
- Extreme Engineering Solutions – Power Architecture processing and development chassis
- GE Intelligent Platforms – Power Architecture and Intel processing module, XMC carrier cards, Ethernet switches, and chassis
- Kontron – Intel processing, GbE switch, and development chassis
- Mercury Computer Systems – Processing modules implementing Power Architecture, Intel, FPGA, and GPU components, digital receivers with A/D conversion, XMC carrier cards, and RapidIO and Ethernet switches
- TEK Microsystems – FPGA processing and A/D converters
- Tracewell Systems – development chassis and deployable chassis

(For a full list, see www.vita.com.)

Continued on page 32

Making decisions for OpenVPX designs

However, despite its design advantages and ecosystem, OpenVPX is not a magic elixir for the instant creation of embedded computing subsystems. Integrating the components from the OpenVPX ecosystem into deployable subsystems still requires expertise that spans both computing technologies and application-specific demands.

First, there is the challenge of subsystem design. To look at just one example, designers working within the OpenVPX standard must decide upon a backplane topology. This decision requires an understanding of intrasystem communications technologies, such as switch fabrics. The decision also involves an understanding of the application's data flow. Given an understanding of both technology and application, the designer can select the best backplane approach. The OpenVPX backplane profile decision will rule some components out, while others remain viable.

In an OpenVPX design, this type of decision is repeated many times within the context of planes, pipes, and profiles. It requires skill and experience to create a subsystem design optimized for maximum performance in a specific application. After that stage is complete, the next step is selecting the best components.

The process of component selection

The market has supplied great depth and variety in available OpenVPX technology components; making the right choices from that variety is a critical part of developing an application-optimized design. While it is often tempting to stay within the "comfort zone" of a given vendor's product line, the only way to deliver maximum value is to carefully evaluate all the options in the ecosystem. For every type of component – backplane, carrier card, power supply, processing module, and so on – it is necessary to compare what is available with what is needed and take a "best-of-breed" approach to selection.

Performance numbers are important to this evaluation but so are SWaP parameters, interface compatibility, software support, reliability characteristics, and environmental limitations. Effective component selection requires a comprehensive understanding of the application's goals, system requirements, and related limitations. As with any complex design activity, experience has great benefits. Mercury was recently involved in a subsystem design effort that illustrates this process.

OpenVPX ecosystem – UAV case study

A UAV platform required an image and signal processor to process, exploit, and disseminate large amounts of multisensor data (Figure 2). New technology for multi-image processing, image compression, and forensic data storage was needed. Achieving SWaP and QRC schedule requirements were also crucial to program success. A determination was made that basing the subsystem design on

Figure 2 I OpenVPX subsystem computing supports a new, multisensor program.

OpenVPX was the best way to unite the efforts of multiple technology vendors and still create a functional, interoperable subsystem on schedule.

Because all the vendors were working from the OpenVPX Specification, a common "language" was used, which greatly reduced the response time from board, chassis, and backplane suppliers. Mezzanine card carrier modules, JPEG compression modules, and new types of processing modules were all selected and successfully integrated into an appropriately sized backplane and chassis combination. After successfully completing initial field tests, this program has moved on to the next phase.

OpenVPX is ready to support next-generation programs

The DoD is committed to driving more programs that rapidly deploy advanced capability in support of the warfighter; one result of this commitment is a need for powerful, integrated embedded computing subsystems built on a standards-based, robust ecosystem.

The OpenVPX standard, with its focus on component interoperability, offers a solid basis for faster, less risky development of the complex, new subsystems that will meet these demands. Using the OpenVPX concepts of planes, pipes, and profiles, system architects and designers can define technologies that are optimized to satisfy a specific set of application requirements and also have unambiguous parameters for component interoperability.

More than 30 vendors have produced components that adhere to OpenVPX, creating a solid and rapidly growing ecosystem that supports OpenVPX designs. Ecosystem choices include multiple styles of processing modules, mezzanine carriers, storage cards, I/O interfaces, fabric switches, backplanes, and chassis. After developing an optimized design, subsystem developers must carefully evaluate and select the best possible components from this available ecosystem.

A combination of an optimized OpenVPX design and effective component selection gives developers a flexible but reproducible process for the creation of next-generation embedded solutions.

Reference:

[1] "Vice chief: FCS vehicles will transform warfighting," by John R. Guardiano, Army News Service, Oct. 8, 2008, www.army.mil/-news/2008/10/08/13149-vice-chief-fcs-vehicles-will-transform-warfighting

Thomas Roberts *is a Solutions Marketing Manager at Mercury Computer Systems. He has more than 25 years of experience in systems engineering and technical marketing with IBM, Nixdorf, Data General, Digital Equipment, and Compaq. He holds a BS in Engineering from Cornell University and an MBA from the University of Kansas. He can be contacted at troberts@mc.com.*

Mercury Computer Systems
978-256-1300
www.mc.com

The future of rugged COTS: A 30-supplier OpenVPX ecosystem supports VPX-based systems

By Vincent Chuffart

A plethora of VPX (VITA 46) specifications prompted the need to develop a framework for system-level interoperability. Hence, OpenVPX interoperability is now in place, and its ecosystem is already maturing with products such as test backplanes, test equipment, and much more. With an experienced group of suppliers offering a variety of OpenVPX compliant technologies, the question is not if a military system designer will initiate a VPX-based application, but when.

U.S. Navy photo by Mass Communication Specialist 2nd Class Adrian White

VME has been the standard-bearer in rugged COTS military systems for quite some time. Developers have enjoyed unequaled flexibility, thanks to VME's open architecture, proven reliability, and vast ecosystem. However, today's systems designers need embedded computing technologies to handle the massive increase of data – as much as 10 times more – to be processed from advanced sensors. System designers also need to integrate enhanced radio communications with radar and other imaging systems powered by high-performance processors and chipsets. VME progeny VPX (VITA 46)-based platforms are the successor in helping designers achieve these goals.

Additionally, OpenVPX (VITA 65) is a major milestone in providing the necessary broad-based system-level-interoperability and resultant ecosystem for the modular serial switched backplane designs enabled by VPX. More than 100 compatible products from more than 30 suppliers are "at the ready" to support VPX-based military systems with a powerful combination of greater performance and lower Size, Weight, and Power (SWaP). This array of new rugged COTS VPX-based technologies has cleared the path for widespread OpenVPX adoption.

Building a sturdy foundation for VPX

VITA working groups have collaborated to secure the viability of the VPX standard by giving it a sturdy foundation. This foundation includes three important specifications: VPX/VITA 46, the board-level base electrical and mechanical standard; VPX-REDI/VITA 48, an enhanced mechanical ruggedization format; and OpenVPX/VITA 65 for system-level VPX interoperability. A major advantage of the board-level specification is that it will allow a steady and competitive ecosystem of connectors and backplanes to emerge. The defense market should realize the same benefits achieved with VME, such as the ability to secure a low-level mechanical and backplane signal interface. Without this secured foundation, it would not have been possible to future-proof VPX platforms.

While it is not expected that customers will start mixing boards from multiple suppliers in their first experience with VPX, OpenVPX is an achievement that will guide all VPX board, backplane, and computer designs from now on. It provides the needed framework for a reliable and continuous technology insertion approach, which is the very the essence of backplane-based computing systems as compared to limited, closed black-box designs. OpenVPX will also allow integrators to design boards to address specific application requirements that they can trust to be compatible with the ecosystem for many years to come.

Elements of a vigorous ecosystem

A healthy OpenVPX ecosystem requires a versatile offering of hardware components that includes backplanes and custom backplanes as well as boards and systems,

software and operating systems, design tools, and other elements. Because VPX is based on point-to-point, high-speed links and not a parallel bus, designers need specific backplane routing to implement the most effective computing solution.

On top of the existing OpenVPX profiles that define backplanes slots and boards, a generic set of computer profiles will emerge. These profiles match the most popular application domains, like safety-critical computing, high-performance parallel computing, or embedded SBCs with multiple I/O boards as shown in Figure 1. Within the same computer profile, generic backplanes will become apparent, fostering reuse of the same backplane in multiple designs. Board suppliers such as Kontron are partnering with other suppliers to offer a complete family of generic backplanes.

Hybrid solutions combining legacy VME boards with leading-edge processor cores are also being implemented to meet specific market demand and help guarantee a smooth migration path to OpenVPX. Figure 2 illustrates one migration path option.

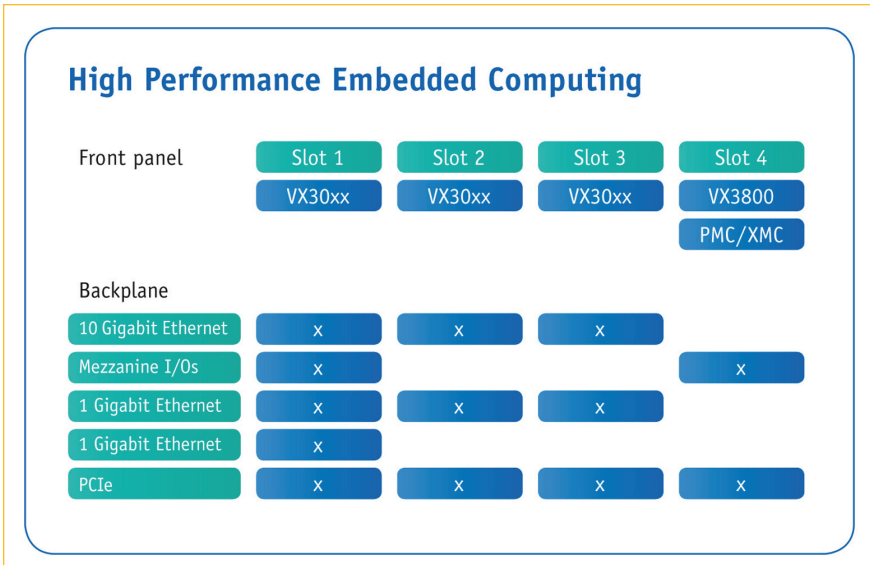


Figure 1 | Generic VPX profiles for high-performance computing, in addition to OpenVPX system specification profiles, enable reuse of the same backplane for multiple designs.

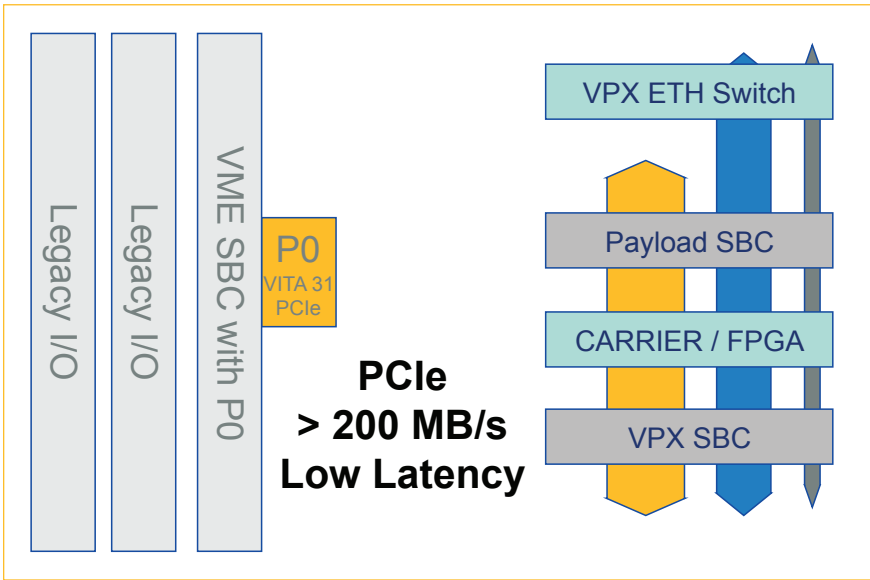


Figure 2 | A 3U VPX heterogeneous backplane solution from 6U VME to 3U VPX is a migration path that addresses legacy VMEbus and software.

Military system designers will most likely evaluate the quality of the VPX technologies based on whether the board supplier also proposes a viable and compatible software road map. With software, there are two main aspects to consider: moving data on the backplane and managing the computer health.

Moving data

Companies will move data via their preferred data plane serial link technology, and data pipes have been predefined by OpenVPX. The clear winners based on the recent VITA OpenVPX survey appear to be PCI Express (PCIe) and Serial RapidIO, with 10 GbE looming in the not-so-distant future. PCI Express is a plug-and-play, cost-effective hardware approach to data transmission and can be used to build very fast static routing crossbar topologies that are well-adapted to parallel multiprocessing found in many electronic warfare applications. An important consideration is price versus performance. A low hardware price tag is attractive, but may not seem like a deal when engineering resources spend many months trying to implement very complex code at the silicon level to achieve the simplest things such as organizing data flows on the backplane.

> “One of the first VPX benefits to military system designs is the opportunity to reduce size. To date, the physical dimensions of 6U VME-based systems could not take advantage of the reductions achieved from 10 years of silicon process and density advancements.”

Health management

In most current VME deployments, health management is handled within low-level application code that is not vendor agnostic. This is why a VITA 46.11 subgroup is working on universal VPX health management that builds on the SMB signals implemented in VPX backplanes. The first successful VPX suppliers to offer a complete solution will likely be the ones who can leverage their experience from other industries such as telecommunications to provide a comprehensive approach to remote computer management. Designers should engage with proven suppliers who can offer software APIs designed for health management for existing applications running on VPX SBCs.

Applying the OpenVPX ecosystem to VPX designs

One of the first VPX benefits to military system designs is the opportunity to reduce size. To date, the physical dimensions of 6U VME-based systems could not take advantage of the reductions achieved from 10 years of silicon process and density advancements. For an application such as an airborne situational awareness system, size also equates to weight, power consumption, and hence mission time. With VPX, very powerful computers can be designed using 3U boards – a significant change thanks to a viable OpenVPX ecosystem.

Payloads in a UAV situational awareness application include video, radar, Electro-Optical/Infrared (EO/IR), and Electronic Countermeasures (ECM), which forces designers to balance performance and SWaP issues. These payloads demand higher-performance processing for differential signal processing. Once again, VPX comes through with higher multi gigabytes per second of data bandwidth at the backplane. Newer radar applications are designed to see finer details, extract tiny bits of information from noise, or detect objects or people at a farther distance. Using VPX for this application satisfies the requirement to move more data within the computer, not just offer more processing power.

For this kind of airborne image application, it is important to select the right components to handle signal processing and to process, exploit, and disseminate large amounts of multisensor data. Interoperability and a multisupplier approach are crucial to achieving SWaP, satisfying aggressive program deployment schedules, and meeting DoD mandates for the use of open standards.

An OpenVPX compatible 3U VPX board is an excellent choice for such an airborne imaging system. A SATA SSD storage solution fits well with this application, as does the integration of an OpenVPX-based XMC interface. This would allow the needed I/O to the backplane – a raw video stream for a high-definition camera can reach 400 MBps – as well as utilizing PCIe connectivity to deliver next-generation radar and full-motion video capabilities. Ground systems can tap into compressed, live video or other information that is easily handled by VPX-based platforms. These platforms provide higher-performance processing per slot and also higher-speed interconnects between processing and I/O elements using PCIe, 10 GbE, or Serial RapidIO. Another benefit of VPX is that it can be used to implement codecs such as ITU-T H.263, H.264 (MPEG-4 part 10) and JPEG2000, efficiently allowing software encoding on general processor boards.

A ruggedized VPX conduction-cooled board with a 0.8-inch pitch is also a good choice in this space-constrained application. Interestingly enough, the results of the recent VITA VPX survey indicate that a significant proportion of VPX planned deployment will be conduction-cooled designs. And, because the technology features of the different ecosystem elements are only part of the equation, interoperability also ensures high availability and reliability for this airborne application.

Vincent Chuffart *is Product Marketing Manager at Kontron. He has more than 20 years of experience in computer software and hardware development, and is responsible for military product management at Kontron. Previous experience includes the EU EUROPRO parallel signal processing computer project and specifications of multiple generations of CETIA and Thales Computers SBCs. He can be contacted at vincent.chuffart@kontron.com.*

Kontron
888-294-4558
www.kontron.com

OpenVPX Product Spotlights

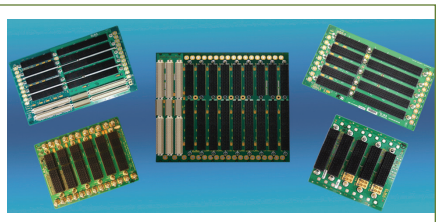
VPX6-187 6U OpenVPX™/ VITA-65 Freescale QorIQ™ P4080 Single Board Computer

- Freescale QorIQ™ P4080 Communications Processor with eight Power Architecture™ processor cores at up to 1.5GHz
- Up to 4 GB DDR3 SDRAM controlled by dual 64-bit controllers
- Full complement of I/O capability (Ethernet, serial, USB 2.0, 1553, Serial ATA, TTL and differential discretes ...,)
- One PMC/XMC site supporting parallel PCI and PCI Express and one XMC site with full complement of XMC I/O
- VPX/OpenVPX/VPX-REDI formats with up to six 4-lane fabric ports

CURTISS WRIGHT Controls Embedded Computing

Curtiss-Wright Controls Embedded Computing
703-779-7800
www.cwcembedded.com

OpenVPX Backplane & Accessory Family

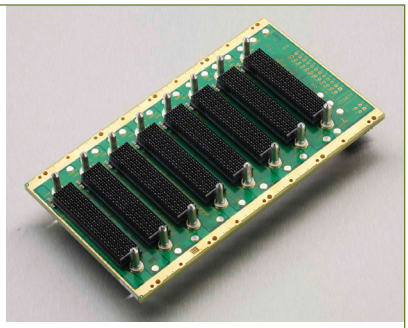


- Largest family of OpenVPX/VPX Backplanes & Accessories in the industry
- 3U, 6U, and 6U Hybrid versions to VITA 46 and VITA 65 specifications
- Pre and post design simulation and characterization services
- VPX load boards, extender boards, RTMs, and SerDes test modules
- VPX cabling solutions and test backplanes

bustronic Elma Bustronic

Elma Bustronic
510-490-7388
www.elmabustronic.com

3U VPX Backplane



- 3U 8 Slot VPX Backplane (6 Payload Slots, 2 Switch Slots)
- Dual Star X4 configuration; 5 HP from slot to slot (25.40 mm)
- Compliant to VITA 46.0 baseline specification, supports VITA 65/OpenVPX
- M3 studs and ATX connector for power entry
- PCB size 128.5 mm x 229.4 mm x 5.4 mm

HARTMANN ELEKTRONIK A Phoenix Mecano Company

Hartmann Electronic
937-324-4422
www.hartmann-electronic.com

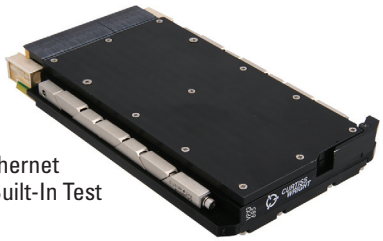
MPMC-9351 OpenVPX™/ VITA-65 Multi-Platform Mission Computer System

- Fully qualified ruggedized system ready for field deployment
- Optimized for SWaP (Size, Weight and Power) constraints
- Packaged COTS (PCOTS) subsystems comprised of state-of-the-art components from our embedded computing library
- Faster deployment, lower development costs and reduced program risk
- US eyes only and ITAR-free models available

CURTISS WRIGHT Controls Embedded Computing

Curtiss-Wright Controls Embedded Computing
703-779-7800
www.cwcembedded.com

VPX3-685 3U OpenVPX™/ VITA-65 Secure Ethernet Router

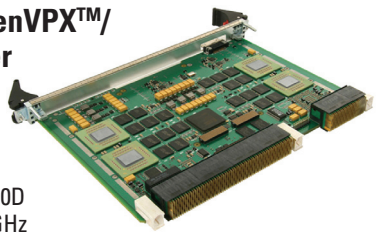


- Fully managed L2/L3 Ethernet router with extensive Built-In Test (BIT) features
- Flexible port configurations to rear VPX
- Enhanced security processor with extensive secure software support
- Fast boot configurations
- Declassification capability for secure erasure

CURTISS WRIGHT Controls Embedded Computing

Curtiss-Wright Controls Embedded Computing
703-779-7800
www.cwcembedded.com

CHAMP-AV6 6U OpenVPX™/ VITA-65 Quad Power Architecture DSP Engine



- Quad Freescale Power Architecture™ 8640/8640D processors at up to 1.0GHz
- Up to 1 GB DDR2 SDRAM with ECC per processor
- Serial RapidIO dataplane interface
- One XMC site supporting PCI Express
- Gigabit Ethernet to all processors with on-board switch

CURTISS WRIGHT Controls Embedded Computing

Curtiss-Wright Controls Embedded Computing
703-779-7800
www.cwcembedded.com

INNODISK®
Beyond your imagination

EverGreen

Industrial Flash Storage

- Highly Cost-effective SSD solution
- 30 times lifespan prolonged
- Improved 100 times IOPS/Random write performance
- WAI close to Zero
- Enhanced reliability by fewer swapping
- SMART functions support for all evergreen products
- Energy Saving and Carbon Reduction

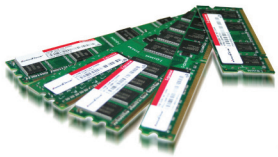
The total solution for Memory and Flash Storage

SSD Industrial Solid State Disk

2.5" SATA 20000
Capacities: 16GB~256GB
Read:230MB/s(max.)
Write:160MB/s(max.)

1.8" SATA 10000
Capacities: 8GB~64GB
Read:160MB/s(max.)
Write:140MB/s(max.)

i-DIMM Series



-40°C~+85°C Wide Temp. Available

Low Profile Available

Embedded Solution:
Low Profile, Wide Temp.
Server/Workstation Solution:
w/ECC, w/ECC w/PLL, w/ECC w/R
Printer Solution

PCIe Solid State Disk
Matador Series

Capacities: 128GB-512GB (SLC)
128GB-1TB (MLC)
Read: 900MB/sec.(SLC)/700MB/sec.(MLC)
Write: 550MB/sec.(SLC)/500MB/sec.(MLC)

8000 Series-EDC/iCF

-40°C~+85°C Wide Temp. Available

Vertical type 40pin
Capacities: 2GB~16GB

iCF 8000
Read: 80MB/s(max.)

iCF Write Protect Series
Write: 75MB/s(max.)

Mini PCIe SSD

Capacities: 4/8/16/32GB
Read: 160MB/sec.
Write: 140MB/sec.

SATADOM

-40°C~+85°C Wide Temp. Available

Low Profile / Vertical Type
Capacities: 128MB~8GB
Read: 24MB/s(max.)
Write: 14MB/s(max.)
Dimension: 0.81x1.54x0.31(inch)
Dimension: 0.90x1.28x0.31(inch)

www.innodisk.com

InnoDisk USA Corporation
43130 Osgood Road, Fremont, CA 94539 TEL: 510-314-8393 FAX: 510-314-8394 Email:usasales@innodisk.com

Executive Speakout

Avnet enables higher levels of integration

By David Moore, Director, Business Development
Defense/Aerospace, Avnet Electronics Marketing

At the recent AUVSI unmanned vehicle systems conference in Denver, it was evident that a shift in protocol was taking place. With over a dozen embedded computing suppliers present – each touting their latest version of FPGA- or DSP-centric, single board solutions – it was clear that they were out to catch the eye of the defense subcontractor community. Continuing their migration towards outsourcing embedded board solutions, the defense subcontractor community is choosing to integrate, rather than design, this portion of their electronic subsystem. Whether it is cost, obsolescence, efficiency in design, or all three – an opportunity has opened for embedded computing in the defense sector.

Small form factor boards, conducive to Size, Weight, and Power (SWaP) reduction requirements, were on display everywhere at the conference. Standard small form factors like COM Express™, equipped with a very low power consumption Intel® processor and Mini-ITX, are helping to make a viable argument to support the selection of embedded boards for the next generation of smaller, unmanned vehicle systems. Keeping in mind that the average soldier currently carries between 20 and 40 pounds of batteries to fuel his array of technological devices, significant value is evident in the reduction in power consumption for soldier-carried electronics.

The defense and aerospace industry is also using custom embedded solutions, such as System in Package (SiP), for further SWaP reduction (Figure 1). SiP can accommodate ASIC and/or FPGA technologies by utilizing a variety of microelectronic packaging techniques resulting in significant SWaP reduction. Utilizing these packaging methods allows for certain semiconductor functions to be embedded into the board substrate. Die can also be packaged via flip chip, or an ASIC can be utilized to replace many of the individual component functions – meeting our military's objective to create more affordable and precise intelligent munitions.

For more than 50 years, Avnet had established a trusted relationship with the defense industry by providing the latest in semiconductor technologies and agnostic component selection to our customers. Once considered predominantly a solution for next-generation communication systems, COTS/MCOTS are now widely accepted in an extended variety of military applications including navigation control and target acquisition systems on current UAV platforms. The new concept or next-generation product design cycle is not the only opportunity for embedded computing in the defense sector. The ongoing demand for the production of combat-proven legacy systems, such as sectors of our current military missile arsenal, is in direct contrast with the reality of commercially driven semiconductor obsolescence. All military electronic subsystems have a saturation point, when end-of-life component issues drive redesign. Some of these redesign projects are relying on outsourced embedded computing hardware driven by in-house proprietary software as the best path towards meeting their requirements.

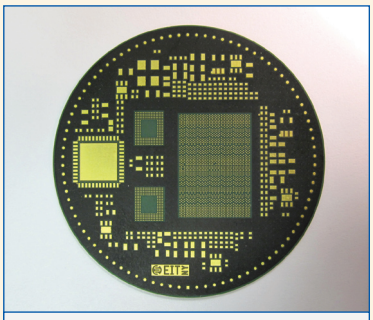


Figure 1 | System in Package (SiP), courtesy of Endicott Interconnect

Avnet continues to develop design and supply chain services to meet the evolving needs of our customers in the defense, aerospace, and civil aviation markets.

Avnet Secure Micro Solutions aligns the core strengths of Avnet Electronics Marketing, Endicott Interconnect, and IBM Microelectronics. Avnet provides ASIC/FPGA design experience and proven supply chain solutions for the defense community. Endicott provides DMEA trusted substrate/module packaging and a turnkey technical solution for SiP. IBM is the world leader in semiconductor technology: Si, SiGe and provides DMEA trusted design and foundry.

Avnet Embedded extends our legacy engineering expertise from component design and selection assistance to filtered COTS/MCOTS selection to subsystem integration. This Avnet team provides the defense subcontractor community with current knowledge about the latest embedded processing platforms, related peripherals, and operating systems. In addition, the highly skilled team of Avnet Embedded system architects has significant experience helping defense customers select and implement the right combination of hardware and software to meet stringent DoD/DoHS requirements. Finally, Avnet Embedded supports customer product development with a comprehensive suite of integration services.

Avnet Electronics Marketing **www.avnet.com**

MIL/COTS DIGEST

The Defense Electronic Product Source

October 2010

In This Issue

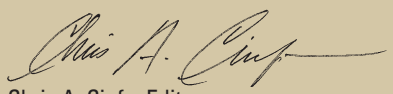
YOUR ATTENTION PLEASE

As I write this in mid September, Intel has taken the wraps off its next-gen CPU architecture called Sandy Bridge and disclosed the addition of eight new Atom processors for embedded. As well, Freescale just said it would add the vaulted AltiVec vector processing engine to select QorIQ CPUs in the near future. Things are certainly heating up in the CPU race – and Freescale may well be a contender again in the Aerospace and Defense (A&D) market.

Speaking of heat, it's nearly always a problem in A&D applications (along with cold temperature, shock, and vibration). "Rugged" boards and systems form the basis of this issue's collection of New Products. We've got a chassis designed for deployment as a ready-to-go Mission Computer that can be configured with 3U modules in CompactPCI, VPX, or OpenVPX.

There are three 3U CompactPCI boards, available in either conduction- or air-cooled versions and equipped with Freescale QorIQ, Intel Core i7, or communications processors. You'll also find two PMC or PMC/XMC modules, both of which are designed for mass storage and equipped with HDDs that withstand big-time shock and vibration. Finally, there's a 6U CompactPCI SBC with the big daddy Core i7, and even a Core 2 Duo-equipped COM Express board.

It's so exciting to see the latest COTS technology CPUs and form-factors all dressed up and reporting for service. Ten-hut!



Chris A. Ciufo, Editor
cciufo@opensystemsmedia.com

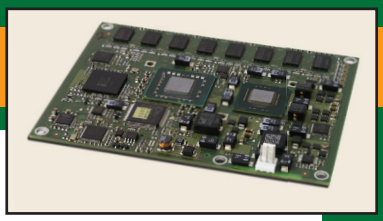
Reporting (fully qualified) for field deployment

Integrated into ruggedized enclosures, MPMC-935x Multi-Platform Mission Computer Systems are fully qualified for field deployment. System components come from the Curtiss-Wright embedded computing library. Custom configurable, the 3U five-slot systems are described by the company as Packaged COTS (PCOTS) subsystems. In addition to supporting CompactPCI, MPMC-935x Misson Computer Systems support VPX and OpenVPX. Other configurable system variants are available. System design takes Size, Weight, and Power (SWaP) constraints into consideration. According to the company, these systems help developers mitigate the risk linked to hardware and software development and certification tasks. NRE costs shrink significantly because PCOTS products leverage fully developed system solutions. Also avoided are issues with incompatible drivers, backplane issues, or BSP versions, says Curtiss-Wright, because it ensures that all boards and software work together.

www.cwcembedded.com

CURTISS-WRIGHT CONTROLS EMBEDDED COMPUTING

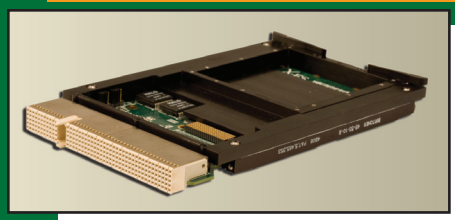
Rugged COM Express board



Developers seeking a small form factor board that targets harsh environments where space is at a premium (think unmanned vehicles) now have the bCOM2-L1100 to consider. Manufactured with soldered components for reliability, the bCOM2-L1100 has an Intel Core 2 Duo processor operating at up to 2.26 GHz and up to 4 GB of soldered DDR3 SDRAM. Connectivity and I/O capabilities include Gigabit Ethernet, eight USB 2.0 ports, four Serial ATA (SATA) ports (RAID-configurable), one PATA port, eight GPIO ports (four in, four out), one LVDS port, two SDVO channels, VGA, High Definition Audio (HDA), and PCI Express (one 4x PCI Express lane or four 1x PCI Express lanes). Mechanical stand-offs insulate to a high degree against external forces. Extended temperature variants and conformal coating are options.

www.ge-ip.com **GE INTELLIGENT PLATFORMS**

3U CompactPCI module with Freescale eight-core P4080 processor



Intelligence, Surveillance, and Reconnaissance, Extreme Engineering Solutions (X-ES) would like you to meet a 3U CompactPCI single board computer with extended shock and vibration tolerance based on the Freescale QorIQ P4080 processor, the XPedite5430. The P4080 processor has eight 1.5-GHz Power Architecture e500 cores and joins an XPedite5430 feature set that includes: two channels of up to DDR3-1333 ECC SDRAM up to 8 GB (4 GB each); up to 16 GB of NAND flash and 256 MB of redundant NOR flash; x4 PCI Express or Serial RapidIO interfaces; two Gigabit Ethernet ports; two serial ports; and two USB ports. OS support includes Green Hills INTEGRITY Board Support Package (BSP), Wind River VxWorks BSP, and Linux BSP. Like the earlier 5470 X-ES P4080-based module, it meets MIL-STD-810F.

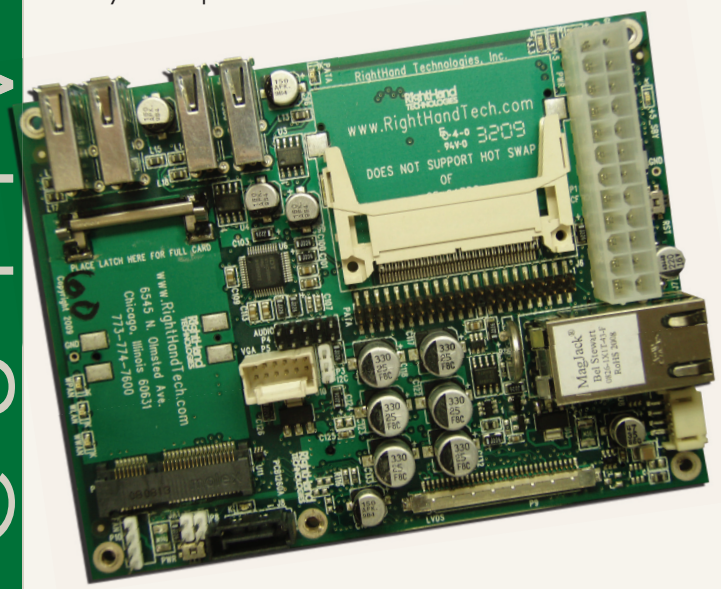
www.xes-inc.com **EXTREME ENGINEERING SOLUTIONS**

COM Express improves time-to-market for embedded computing

By Steve Valentor, President

Product engineering is expensive. While creating exciting new products is critical to moving your business forward and staying ahead of the competition, the decision to invest in a new development is often difficult. Add in the fact that technology improvements will make your design obsolete in a few years, and the decision becomes daunting.

Now consider the advantages of design using the COM (Computer-On-Module) Express standard architecture, enabling a highly integrated embedded PC with an industry standard interface. By developing a custom COM Express carrier board to complement a processor module, product engineers can create application-specific hardware with a flexible, modular design to support graphics, signal processing, video, networking, USB, storage, audio, various other I/O functions and a variety of other expansion interfaces. Perhaps most importantly, the design of the high-speed, compact, difficult-to-layout, highly timing-sensitive CPU-memory subsystem is independent from the design of the carrier. The unique set of peripherals needed for your specific application resides on the carrier board. Where it may take a full year to design a CPU module, a custom carrier can be completed in weeks. COM Express ensures that the BIOS, operating system, tools, and basic utilities are available and work. Device drivers and applications can easily be adapted to the custom carrier.



COM Express builds in flexibility. If your application needs the newest, highest-performance CPU, the COM module can be exchanged for a newer, more powerful alternative. If the entire system needs a new or different peripheral, the carrier can be modified without having to achieve timing closure on the CPU-memory subsystem. COM Express may be the fastest and most flexible way to bring your products to market and keep your company ahead of the competition.

While much quicker to design than a multi-GHz processor module, a custom carrier board for military/aerospace applications is not a trivial design task. To take advantage of the flexibility of the design element reuse that COM Express enables, an engineering team must understand the standards and have the experience to design for difficult-to-achieve agency approvals. RightHand Technologies has just such a team and the experience for these demanding markets.

With more than 25 custom carrier projects to its credit – many having been done with RadiSys' COM Express modules – RightHand Technologies has the expertise to provide a full spectrum of embedded design services in the engineering disciplines of electronics, software and mechanical, as well as program management, system integration, formal verification, testing, qualification, certification, manufacturing, supply chain and life cycle management.

RightHand Technologies also can support a quick start of your development efforts with its newly released RCB-122B development board. The RCB-122B serves as both a development platform and reference design for developing your custom I/O subsystem. The RCB-122B, which can be a proof-of-concept vehicle or a full production platform, is available today and can be ordered at www.righthandtech.com/com-express-carrier-board.php.

RightHand Technologies can guide you from the RCB-122B standard product platform to a custom carrier project by helping to evaluate your requirements, drafting specifications, generating schematics and layouts, coding custom FPGA logic, designing custom software, building prototypes, integrating electro-mechanical functions, facilitating agency approvals and manufacturing to exacting standards – all under the watchful eye of an experienced program manager who will report to you each week with a fully transparent status of milestones and deliverables.

RightHand Technologies provides innovative design, specialized manufacturing, and sophisticated functional testing for embedded computing applications for aerospace, defense and other markets. For further information please email info@righthandtech.com.

Steve Valentor joined RightHand Technologies in 2008 as president.

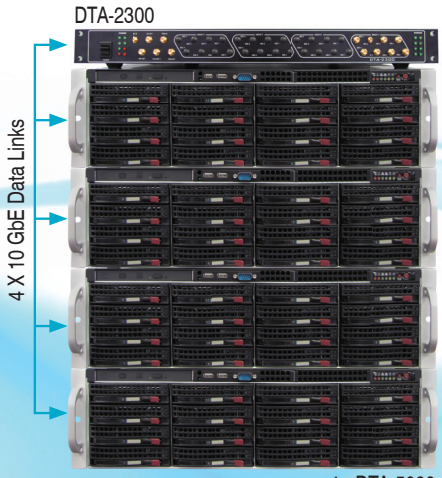
RightHand TECHNOLOGIES

www.righthandtech.com

10G SERIES RECORD & PLAYBACK SYSTEMS

ULTRA-FAST, SCALABLE & 10 GIGABIT NETWORK POWERED

Synchronized (Phase-Coherent) Recording & Playback of Multiple Wideband Radio Signals



10G/R4

- 8 or 16 IF Inputs & Outputs
- 38.4 TBytes Storage Capacity
- 2.4 GBytes/s Sustained Record/Playback Rate
- Optional DTA-3200 (20MHz to 6GHz) tunable RF Front End

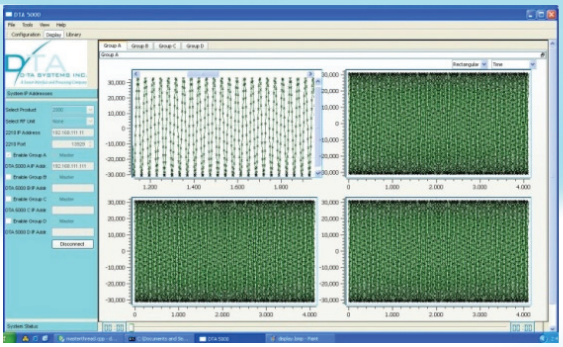
10G/R2

- 4 or 8 IF Inputs & Outputs
- 19.2 TBytes Storage Capacity
- 1.2 GBytes/s Sustained Record/Playback Rate
- Optional DTA-3200 (20MHz to 6GHz) tunable RF Front End

10G/R1

- 2 or 4 IF Inputs & Outputs
- 9.6 TBytes Storage Capacity
- 0.6 GBytes/s Sustained Record/Playback Rate
- Optional DTA-3200 (20MHz to 6GHz) tunable RF Front End

(User PC)



Comprehensive GUI for Failsafe Operation & Control of All System Components. Time, FFT and Waterfall Displays for Monitoring Data Quality During Record or Playback.

With 16-bit 130MHz ADCs & 500MHz DACs and programmable DDCs and DUCs, the 10G Series Systems offer high-precision and large IF Bandwidths. They are fully-integrated for immediate deployment.

1-877-382-3222
SALES@D-TA.COM

Download 10G Series Technical Presentation
WWW.D-TA.COM

NOTHING ELSE COMES CLOSE

D-TA SYSTEMS INC.
A Sensor Interface and Processing Company

SENSOR PROCESSORS THAT DRASTICALLY REDUCE DEPLOYMENT TIME AND COSTS

The AdvancedTCA integration evolution

By John Long

Network-centric warfare is driving the advancement of integrated, open standards-based platforms in the mil/aero industry.

Military applications developers could be excused for pausing to catch their breath after living through dramatic changes for the last two decades. They have seen a large-scale shift away from utilizing proprietary components. Instead to better capitalize on technology, the mil/aero industry began commissioning fully integrated solutions. This change has allowed developers to focus on their value-added services while taking advantage of AdvancedTCA performance attributes.

Historical military equipment development

Historically, the military built its equipment using vertically integrated internal designs. Systems built using inflexible, proprietary components resulted in expensive and lengthy development times and made it difficult to keep up with evolving technologies.

The Network-Centric Warfare (NCW) doctrine introduced, beginning in 1996, a new way of conducting military operations. A fundamental shift away from compartmentalized war machines created a robustly interconnected network of military units that depended on the timely transfer of actionable information for cohesive operation. For equipment manufacturers, this fueled heavy demand for networking and performance capabilities, while reducing the power and space allotments for embedded systems.

Recognizing the inherent limitations of using this proprietary development method, military equipment manufacturers began transitioning to using Commercial Off-the-Shelf (COTS) solutions. Standards-based COTS solutions, such as rugged VME, CompactPCI, and VPX, meant designers chose from the latest computing and networking technologies at reduced costs and cut development time because they were not reinventing the wheel – or hardware. However, NCW performance, bandwidth, and power consumption demands rose sharply and soon surpassed the capabilities of the traditional military standards, forcing developers to look for new approaches.

Addressing ruggedized networking applications

System engineers needed a platform that could meet the unique Size, Weight, and Power (SWaP) demands of highly ruggedized networking applications. Older standards could not satisfy all of these requirements. They found the AdvancedTCA form factor, originally developed for the telecommunications industry, offered a robust, high-performance, fault-tolerant platform that was easily customized for a variety of compute-intensive applications.

- **Open standard:** As an open standard, AdvancedTCA offers a smooth upgrade path and broad supplier base, eliminating the risk of product obsolescence.
- **Robustness:** AdvancedTCA offers field-proven robustness as it is designed to withstand the more extreme environmental factors, including shock, vibration, and G-forces.
- **Carrier-grade reliability:** AdvancedTCA provides hardware redundancy at every level, including fans, power entry modules, backplane data, and shelf managers, as well as fault tolerance on an application level for mission-critical applications.
- **Power efficiency:** AdvancedTCA's low power consumption allows it to meet application requirements for power efficiency and heat dissipation.
- **Scalability:** AdvancedTCA is fully scalable and customizable to comply with a range of application requirements.
- **Performance:** AdvancedTCA offers significant performance advantages over other open standards-based COTS products, with a larger board size affording developers more area for processors, chipsets, memory, and graphics processor units.
- **Interoperability:** AdvancedTCA common form factor blades allow designers to create multiple applications and network elements on a standard architecture while providing maximum flexibility with multi-vendor interoperability from AdvancedTCA's solid and mature ecosystem.
- **Bandwidth:** AdvancedTCA technologies can fully support 10 Gb of traffic on the system backplane to process voice and video traffic. And PICMG is proceeding with standards work to create a 40 Gb specification to aid multivendor interoperability of system elements.

"Defense primes recognized that ATCA's attributes fit well with modern military networking requirements," explains Bill Rick, director of federal sales, Astute Networks.

Systems engineers began using AdvancedTCA for a variety of military applications, beginning with aerospace then moving to ground- and naval-based applications. Engineers worked on the system-level integration and proceeded to write software for AdvancedTCA-based applications, thus realizing the possibilities that AdvancedTCA offered for interconnected military operations.

Integrated solutions for mil/aero

Manufacturers such as RadiSys recognized the need for integrated platforms for mil/aero applications. Pre-integrated AdvancedTCA platforms offer a number of benefits for system developers. The pre-integrated platform approach gives developers greater choice in selecting the level of engagement needed on a project basis. This allows manufacturers to capitalize on AdvancedTCA's interoperability with a consistent architecture that developers can use to support a variety of applications. Using pre-integrated platforms offers third-party validation, ease of maintainability, and a single point of

responsibility for system integration. Finally, the pre-integrated approach significantly reduces time-to-market without increasing project risk; in some cases, this means moving from concept to field deployment in a few months rather than years. Based on these overwhelming advantages, integrated platforms are becoming the new industry building blocks.

A rugged platform for mobile command and control

To meet the evolving requirements of integrated computing, RadiSys developed the C2 Server (Figure 1), the industry's first rugged AdvancedTCA platform for mobile command and control. The C2 Server is a straight out-of-the-box solution that can be quickly deployed in the field. Integrated computing, switching, and storage are included in one platform. The C2 Server offers higher performance with 33 percent less weight and lower power consumption than comparable Rack Mount Servers (RMS), features that facilitate mobile computing.

Figure 1 | The C2 Server from RadiSys has arrived as the first rugged AdvancedTCA platform for mobile command and control.

This pre-integrated RadiSys platform leverages best-of-breed technology from key industry players Astute Networks, LCR Electronics, and RadiSys. RadiSys' Promentum ATCA-2210 switch is the industry's first 10 Gigabit (10 GbE) capable switch and control module. Developed as part of an AdvancedTCA platform, the module's highly integrated, centralized common equipment functions include switching, shelf management, network timing, and system management.

RadiSys Promentum ATCA-4500 series processor blades offer a range of high-performance options for a variety of application needs. The board supports multiple storage functionalities, such as Dual User Flash of up to 16 GB per blade. SSD Advanced Mezzanine Card (AdvancedMC) is also supported by the ATCA-4500 series, which includes optional Rear Transition Module (RTM) support of an additional drive. The boards are designed to meet stringent thermal testing and vibration requirements for mil/aero applications and NEBS requirements for communications applications.

The C2 Server employs Astute Networks' Caspian R1100 storage blades. System capacity ranges from 3.6 TB to 6 TB per AdvancedTCA slot, with its iSCSI offload ASIC enabling a combination of performance and low-power consumption features unique to Astute Networks' AdvancedTCA products.

"Astute Networks' storage solutions offer customers the highest density storage available in a blade format," said Rick.

The C2 Server chassis is from LCR Electronics, which develops extreme rugged enclosure products. LCR designed the chassis from scratch to withstand the most extreme military environments. LCR Electronics' products go through rigorous trials, including temperature, shock, vibration, and severe acceleration testing. Many of LCR Electronics' products have a life cycle of 20 or 30 years.

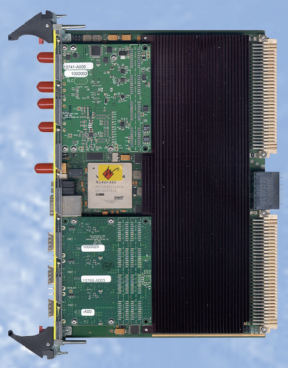
"Our products are uniquely designed to meet the requirements for military

Annapolis Micro Systems

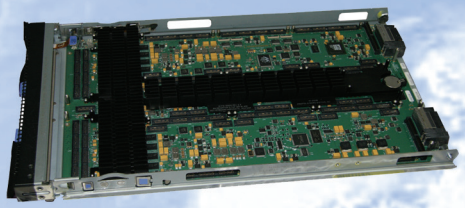
The FPGA Systems Performance Leader

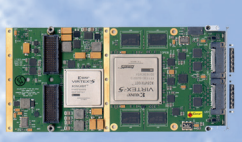
High Performance Signal and Data Processing in Scalable FPGA Computing Fabric

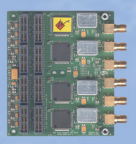
GEOINT, Ground Stations, SDR, Radar, Sigint, COMINT, ELINT, DSP, Network Analysis, Encryption, Image Processing, Pattern Matching, Oil & Gas Exploration, Financial Algorithms, Genomic Algorithms

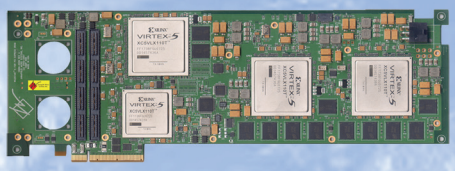


Direct Seamless Connections with no Data Reduction
Between External Sensors and FPGAs
Between FPGAs and Processors over IB or 10GE
Between FPGAs and Standard Output Modules
Between FPGAs and Storage Arrays









Annapolis Micro Systems

Ultimate Modularity
From 1 to 8 Virtex 4, 5 or 6 FPGA/Memory Modules
Input/Output Modules Include:
Quad 130 MSPS thru Quad 550 MSPS A/D
1.5 GSps thru 5.0 GSps A/D, Quad 600 MSps D/A,
Dual 1.5 GSps thru 4.0 GSps D/A
Infiniband, 10G, 40G or 100G Ethernet or SFPDP

VME/VXS/VPX, IBM Blade, PCI-X/PCI Express, PMC/XMC, MicroTCA

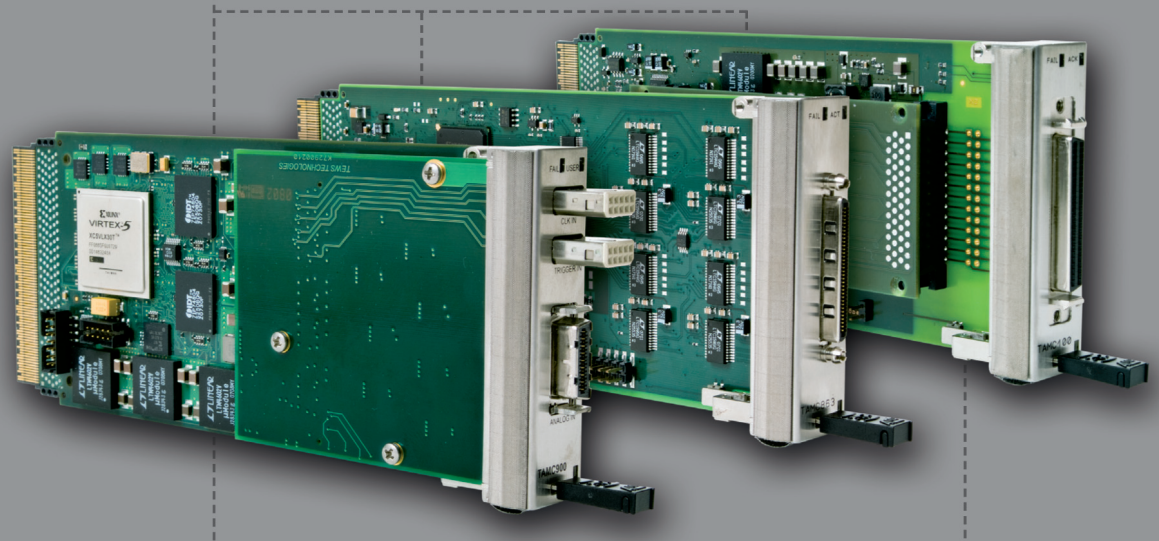
No Other FPGA Board Vendor Streams This Volume of Data Real Time Straight Into the Heart of the Processing Elements and Then Straight Back Out Again

190 Admiral Cochrane Drive, Suite 130, Annapolis, Maryland USA 21401
wfinfo@annapmicro.com USA (410) 841-2514 www.annapmicro.com

I/O Solutions for µTCA™/ATCA®

Mezzanine Carriers
- Single Width Single Slot IndustryPack®
- Double Width Three Slot IndustryPack®
- Double Width Single Slot PMC

- For proof of concept
- For fast time to market
- For flexible I/O solutions
- Hundreds of I/O solutions available off the shelf



High Performance I/O
- 8 Channel High Speed A/D data acquisition with FPGA
- 4 Channel Synchronous Serial Interface
- Virtex™-5 based FPGA solutions
- Customer Specials

General Purpose I/O
- Analog I/O
- Digital I/O
- Serial
- CAN
- Fieldbus
- Motion Control
- Customer Specials

Drivers for VxWorks, Linux, LynxOS, Windows, QNX

w w w . t e w s . c o m

TEWS TECHNOLOGIES

TEWS TECHNOLOGIES LLC: 9190 Double Diamond Parkway, Suite 127 · Reno, NV 89521/USA
Phone: +1 (775) 850 5830 · Fax: +1 (775) 201 0347 · E-mail: usasales@tews.com

TEWS TECHNOLOGIES GmbH: Am Bahnhof 7 · 25469 Halstenbek/Germany
Phone: +49 (0)4101-4058-0 · Fax: +49 (0)4101-4058-19 · E-mail: info@tews.com

applications," notes Daemon Heckman, a Product Line Manager at LCR Electronics. "Not only are our products built to withstand the most extreme environments, but they are built to last."

Looking ahead

While AdvancedTCA has already been adopted across several military sectors, a variety of other applications can benefit from this standard, particularly those applications with limited space and power allotments, such as mobile command, control and communication systems.

As the industry evolves, it is continually moving toward smaller, high-performance systems with reduced power consumption. The AdvancedTCA architecture is also low power in nature. As the military continues to reduce its energy dependency, AdvancedTCA-centric systems such as the C2 Server are poised to deliver ready-made energy-efficient solutions.

John Long *is a product line manager at RadiSys, with a focus on AdvancedTCA Single Board Computers and storage. He has more than 10 years' experience in the communication industry holding various marketing, sales, and operational positions with Intel, Dialogic, and AT&T. John has an MBA from Carnegie Mellon University.*

RadiSys
www.radisys.com
John.Long@radisys.com

6U CompactPCI blade has up to up to 3.2 GHz maximum turbo frequency

With the cPCI-6510 blade, ADLINK Technology makes the case for putting the Intel Core i7 processor and Intel QM57 chipset to work on performance-per-watt ratio, four-thread computing capability, integrated graphics, and extensive I/O support. The Intel Core i7 processor integrates the GPU into the processor for better graphics performance. An optional extended temperature range of -40 °C to +80 °C helps make the cPCI-6510 blade suitable for military applications. Another plus for critical applications in harsh environments: All components are soldered on board. The 32 nm Intel Core i7 processor delivers 2.53 GHz clock speed and up to 3.2 GHz maximum turbo frequency. The blade incorporates two PMC sites and DDR3 memory with ECC. A rugged conduction-cooled version of the cPCI-6510 with identical electronic design, the CT-61, is planned.

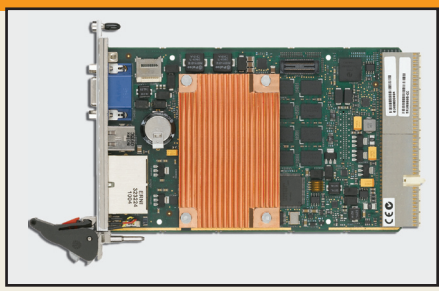
www.adlinktech.com **ADLINK TECHNOLOGY, INC.**

Secure erasing also ends job security for some external hard drives

A high-capacity mass storage mezzanine from Elma aims to put external hard drives or disk modules that require additional backplane slots or external connections out of work. The Elma SecurePMC disk supports 10 major defense agency secure erasure procedures and works on any board with an IEEE 1386.1-compliant PMC site, such as CompactPCI, AdvancedTCA, VMEbus, OpenVPX, and VXS. A front panel push button with an LED indicator shows the data has been securely erased. Write protection takes place via a front panel toggle switch. Extended operating temperature range can be as high as -40 °C to +85 °C, based on user requirements, and the ruggedized mezzanine withstands shock to 1,500 G at 0.5 ms half-sine and vibration to 16.4 G rms (10 Hz to 2,000 Hz random).

www.elma.com **ELMA ELECTRONIC**

F-RAM outperforms flash on new 3U CompactPCI board



Emerson Network Power now brings to circumstances requiring high performance in space-constrained environments a 3U form factor SBC, the CPCI7203. Its integrated Intel Core i7 dual-core processor teams with onboard memory that includes up to 4GB DDR3 and 256 KB non-volatile Ferroelectric Random Access Memory (F-RAM). F-RAM does not require batteries or periodic refreshes. Critical nonvolatile data storage, data logs, and dynamic program updates benefit from F-RAM's ability to run many more read/write cycles and perform faster than flash memory. The CPCI7203 has full hot swap compliance per PICMG 2.1 and supports the PICMG 2.9 System Management specification. Thanks to compliance with the PICMG 2.30 CompactPCI PlusIO specification, the CPCI7203 supports the new serial buses on the J2 connector for data transfer rates of up to 5 Gbps.

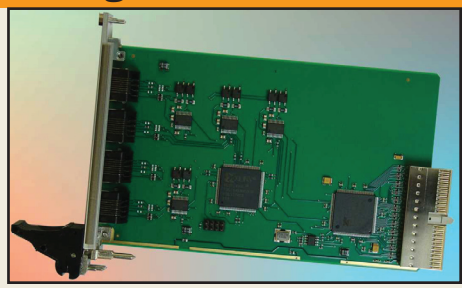
www.emerson.com/EmbeddedComputing **EMERSON NETWORK POWER**

PMC/XMC SATA stands up to shock while mechanical interference stands down

Available in PMC and XMC formats, the SD18 SATA storage modules use either a compact 1.8 inch-hard disk (HDD) or rugged solid state drives (SSDs). Opting for the SSD choice combines the ability to withstand high shock and vibration with up to 160 GB of storage. PDSi notes that whether configured with an economical rotating HDD or with a highly shock-resistant SSD, these low-profile modules fit CompactPCI, AdvancedTCA, VITA 42.3-compatible VME, and PCI Express processor boards without risk of mechanical interference. The onboard 4-port SATA controller makes three additional external drive interfaces possible. In addition to high capacity, these RoHS-compliant modules have a high MTBF (over one million hours).

www.pinnacle.com **PDSI – PINNACLE DATA SYSTEMS, INC.**

3U CompactPCI Serial Communications Controller cuts processing overhead



The TCP467 extended temperature and high-density 3U CompactPCI Serial Communications Controller serial channel has separate 64-byte receive and transmit FIFOs. This significantly reduces the processing overhead that sending data transactions to the transceivers demands. In addition to frugality on the overhead front, this communications controller offers four channels of high-performance RS232/RS422/RS485 selectable serial connectivity. The channels (individually programmable) can operate as RS232, RS422, or RS485 full/half duplex interfaces. Programmable termination for the RS422/RS485 interfaces is possible. Physical connection is via front panel I/O with four RJ45 Modular Jack connectors. Following power-up, all serial I/O lines are in a high impedance state for critical applications. All channels generate interrupts on CompactPCI interrupt INTA, and the UART's Global Interrupt Source Register speeds interrupt source detection.

www.tews.com **TEWS TECHNOLOGIES**

PRODUCT SPOTLIGHT

OM6061 – 1U, 6-slot MicroTCA platform for rugged and intelligent communications

Designed to meet NEBS, the Kontron OM6061 offers six mid-size AdvancedMC slots for multiple system configurations and is pre-tested with the Kontron storage, IA processor, and network processor AMC modules. The three remaining slots are optionally open for a redundant AMC configuration or additional AMC modules, making this platform ideal for security-based communication applications. The OM6061 features an 8-fan, front-to-back cooling set-up, an integrated 360W -48V or -60V power supply and a low-cost MCH module in a 1U, 12.5" deep rack mountable platform. Options available for up to six AM4220 10 GbE Cavium-based AMC modules for a sustained traffic of 120 Gb/s.

kontron

www.kontron.com
info@us.kontron.com

From theoretical to mission-critical: Open standard solutions for tomorrow's mil/aero markets

By Keate Despain,
General Manager, Commercial Business Unit

In the past 10 years, the role of open standards in the mil/aero industry has evolved from a hypothetical solution to an ideal deployment option. Escalating military and aerospace requirements are driving the use of commercial off-the-shelf (COTS) technologies, which provide cutting-edge performance and reduced development time and costs.

Though reliability, ruggedness and longevity are common requirements shared by all applications in this space, the mil/aero marketplace can be divided into three segments, each with different requirements that map to currently available COTS computing technologies. (See Figure 1.)

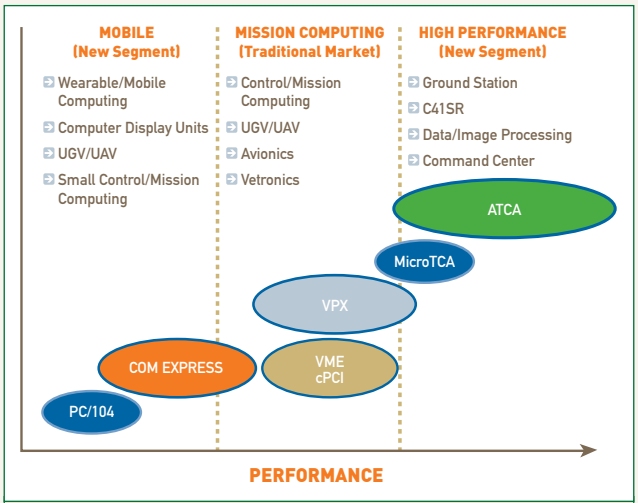


Figure 1 | The mil/aero market's three segments all need reliability, ruggedness, and longevity.

The applications that fall into mission computing, the traditional military market computing segment, are mission controllers, unmanned vehicles, and avionics. These have been well served by VME, CompactPCI, and VPX standards architectures. In recent years, however, the growing scope of military responsibilities, ranging from humanitarian to police and combat operations, has made it imperative to process and distribute greater quantities of data across the globe.

The evolution to what we now refer to as Network Centric Warfare (NCW) means that today, military units must work together cohesively. From the command center to the troops deployed in the field, each independent military unit must share real-time information over highly dependable networks. The movement to NCW has spurred the creation of two new market segments within the mil/aero industry where COTS solutions are making headway.

The first new market segment includes small, mobile applications such as unmanned ground and air vehicles, portable or wearable computers, and computer display units. The ideal standards architecture to serve this market would be, first and foremost, a small form factor with extreme portability. It would also need to perform reliably in the field – under extreme temperatures and vibration conditions. Lastly, any design architecture serving this segment would need to register low power consumption to extend battery life, a critical component to any mobile application.

Offering several small form factor benefits, COM Express, a Computer-On-Module (COM) PICMG standard, meets the need for small size, low power, and excellent performance in space-constrained designs. In addition, developers use COM Express extended temperature designs to satisfy size, power, and performance requirements because the designs can stand up to the rigors of the toughest environmental conditions. Also as the technology life cycle quickens, the COM Express form factor is ideal for inserting new technology without redesigning the entire electronic complex.

The second new market segment is for high-performance applications. Examples of high-performance applications include large systems such as those used in ground control stations, image processing, and command centers. These applications demand high-compute performance and large storage capacity as well as high-bandwidth, low-latency backplane switching to share data across multiple boards.

One board form factor with a proven track record for delivering high performance and high reliability is the Advanced Telecommunications Computing Architecture (ATCA). ATCA also benefits from a large ecosystem with more than five years of deployment experience and widespread adoption. High-performance blades are already available and have been tested to ensure interoperability.

RadiSys brings leading-edge technology to today's standard form factors and offers both ATCA and COM Express solutions. For example, RadiSys' ruggedized ATCA platforms work well for programs such as land mobile communications, aerospace surveillance, and maritime networks that must collect and process large amounts of data in harsh environments. RadiSys' COM Express Extended Temperature products are designed with higher capability components that are rugged enough to handle the toughest environmental factors, yet efficient enough to meet application needs for low power and heat dissipation.

Several standards-based architectures can satisfy the size, ruggedness, and performance requirements of modern warfare including ATCA and COM Express. When performance matters, military and aerospace systems designers are now selecting these next-generation, open standards-based solutions for their future deployments.

Keate Despain is the General Manager of the Commercial Business Unit. Keate joined RadiSys in 2007, after a 12-year career at Intel where he led various groups in the Embedded group focused on communications segment, software, channel management and product marketing. He has also spent several years living and working in China. Keate has a Masters in Business Administration (MBA) from Arizona State University.

RadiSys

www.radisys.com


Dense?
...we take it as a compliment
16 dual redundant fully independent 1553 channels on one ccVME.
EXCALIBUR SYSTEMS
IT'S ABOUT THE SUPPORT
www.mil-1553.com

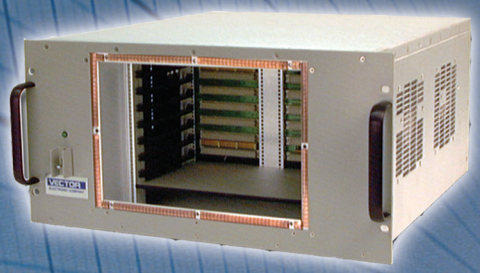
ITAR REGISTERED
NO. M26764

VECTOR

ELECTRONICS & TECHNOLOGY, INC.
A FINE TECHNOLOGY GROUP

VME / cPCI® Ruggedized Chassis

- Well suited for Military / Aeronautics
- VME64x, VME64 or cPCI® compatible
- Mil 461-D, E for shock/vibration, EMI/RFI
- CE and FCC class B, Part 15
- Many power options



790 Chassis

792 Chassis

Series 445, Modified
Full EMI/RFI

VECTOR SPECIALIZES IN:

UNPARALLED FACTORY SUPPORT
CUSTOM CONFIGURATIONS
SHORTER LEAD TIMES

Made in U.S.A

(800)423-5659

www.vectorelect.com

Editor's Choice Products

Editor's note: *Military Embedded Systems is "hip" to the whole Web 2.0 social networking revolution. While we don't know which of today's buzzy trends will last, we're going to start including links to vendors' social networks, when provided. You can also reach us on Twitter, Facebook, and LinkedIn ... and that's just for this week. Next week there'll undoubtedly be more new sites.*

Mission critical on the inside, too

When we think "mission critical," often the first things to come to mind are physical ruggedness … packaging … soldering. But data security is just as imperative. Surely this is what Panasonic had in mind when it partnered with Mobile Armor, Inc. in suiting certain models of Panasonic's rugged notebook Toughbooks with Mobile Armor's DriveArmor data security management, enterprise-class solution.

Accordingly, the Toughbook 19 and the Toughbook 31's new DriveArmor arsenal provides policy-driven control for desktop computers and notebook PCs via 2.5", FIPS-compliant Seagate Technology Momentus self-encrypting disk drives. The DriveArmor data security management solution renders "extensive auditing and reporting capabilities," pre-boot authentication, and centralized management, all to thwart unauthorized data access on stolen or lost computers. Meanwhile, the Toughbook 19 laptop convertible tablet features the Intel Core i5 and a 10.4" sunlight-viewable touchscreen at 1,000 nits and is MIL-STD-810G compliant. The Toughbook 31 rugged clamshell computer features the Intel Core i3 and i5 processor, meets MIL-STD-810G, and features a 1,100-nit, 13.1" touchscreen and IP65 certification.

Panasonic • www.panasonic.com • www.mil-embedded.com/p46271 | Mobile Armor, Inc. • www.mobilearmor.com • www.mil-embedded.com/p46272

Graphical software tool speaks the developer's language

Learning a new language is a difficult, time-consuming, tedious endeavor, whether we're talking about Russian or a new software programming language. And Texas Instruments' C6EZFlo graphical software development tool eliminates this challenge – at least from the software-programming sphere. How? Developers take advantage of the tool's drag-and-drop capabilities when they begin a signal-flow block diagram. Blocks might represent a particular DSP filter kernel or an output/input data transaction, among other items. The tool, in turn, then "generates heavily commented and cleanly structured C code" relevant to that block diagram. The C code can be used as-is or further altered for design changes so you don't need to be an expert on a particular DSP architecture, DSP code, or drivers.

Compatible with TI's C6000 DSP devices and Da Vinci video processors in DSP-based varieties, the C6EZFlo is ideal for fast prototyping of test and measurement applications, as well as industrial monitoring and imaging. Another important benefit, particularly for military designers, is that the block diagrams depicting system signal flow can be used again during migration to additional or different TI DSPs, eliminating a lot of rework.

Texas Instruments • www.ti.com • www.mil-embedded.com/p46273

Continued on page 56

Datacryptor's security stays with the times

To stay relevant, the National Institute of Standards and Technology (NIST) has created and adjusted U.S. security policies for cryptographic modules. First came the Federal Information Processing Standards (FIPS)140-1 Security Requirements for Cryptographic Modules in 1995, superseded by FIPS 140-2, Security Requirements for Cryptographic Modules, in 2001. And with the increase in potential security threats and attacks rising every year, who can blame NIST for mandating these standards for cryptographic modules? One company that has followed NIST's instructions and policies to a "T" is Thales with its Datacryptor network encryptors: Certified to FIPS 140-2 Level 3, users know networks are ultra-secure. (Level 3, one of four FIPS 140-2 levels, adds the dimension of cryptographic modules' physical tamper resistance.)

Other notables about the Datacryptor optical, high-speed network encryptors are that they work with most any optical vendors' wares. They also comprise Ethernet Layer 2 in the following versions: 100 Mbps, 1 Gbps, and 10 Gbps. The optical network encryptors are SONET-SDH based (specifically, OC-3/12/48/192 SONET/SDH), and they are best suited to high-speed commercial and government applications. Additionally, they are ideal for LAN extension, network transport, and satellite communications. Sounds like just what the U.S. DoD could use to keep enemies at bay…

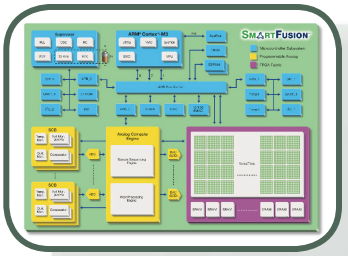
Thales • http://iss.thalesgroup.com • www.mil-embedded/p46274

Activate the clock frequency … but how?

Designing a system is difficult, and finding the optimum clock frequency remains a matter of trial and error. Solving this likely served as impetus for Pentek, Inc. when it developed its Model 7191 Multifrequency Programmable Clock Synthesizer. Incarnated as a PMC module, the user-configurable clock synthesizer renders a high-precision clock source for designers who are developing applications containing D/As and A/Ds. The module also additionally provides custom frequency generation for multichannel DA/AD systems, for example communications and radar applications. And forget about those frequency synthesizers, which are supplanted by the PMC module, eliminating bulk and cost.

Putting it all together: Model 7191 utilizes low-noise VCXOs to generate frequencies; next, a Texas Instruments clock synchronizer shores up common-frequency reference source synchronization. (Of course, the clock synchronizer aims to cut the jitter.) Thus, Model 7191 revs up four configurable VCXO frequencies, along with a quad of divided versions (x2, x4, x8, and x16) pertaining to each oscillator. Five frequencies of these 20 choices can be routed to any of eight buffered 50-ohm outputs. Supporting VxWorks, Windows, or Linux, the PMC module is available on "simple carriers" for VPX (VITA 46), VME, CompactPCI, PCI Express, and PCI.

Pentek, Inc. • www.pentek.com • www.mil-embedded.com/p46275



FPGA offers a triad of wares, all rolled onto a single chip

How much better would it be to combine a triad of components onto a single chip and save integration time and tool cost? Actel's SmartFusion "intelligent mixed-signal FPGA" does just that, by combining a full-featured FPGA, a microcontroller subsystem, and programmable analog onto a single "intelligent" chip. The attention grabber is the "intelligent" aspect. This is provided by the microcontroller subsystem, based on a 100 MHz ARM Cortex M3 processor and additionally sporting 10/100 Ethernet MAC with RMII interface; 16 Gbps throughput communications matrix (multilayer AHB); an External Memory Controller (EMC); a pair of each of 32-bit timers, UART, I^2C, and SPI; and an eight-channel DMA controller.

And as if that weren't enough … the full-featured FPGA utilizes Actel's ProASIC flash-based FPGA architecture based upon 130 nm CMOS featuring densities of 60K to 500K for the system gates, plus 204 I/Os and 350 MHz performance. That much capability frees up board space and lowers the system's overall power consumption. Then there's the programmable analog, powered by the Analog Compute Engine (ACE). ACE offloads analog initialization from the ARM by executing sample computation and sequencing. ACE comprises a trio of up to 600 Ksps sampling ADCs (up to three 12-bit); as many as three 12-bit first order sigma delta DACs; multiple integrated voltage, current, and temperature monitors; and up to ten high-speed comparators at 50 ns. And IP security is no problem, thanks to Actel's FlashLock technology, standard aboard SmartFusion FPGAs.

Actel • www.actel.com • www.mil-embedded.com/p44591

Interceptor bridles the email monster

Hackers beware. There's a new email security compliance enforcer in town and it's coming to a U.S. government agency or enterprise near you: Espion International, Inc.'s Interceptor security-hardened email compliance enforcer. The Interceptor can be enabled with MX LOCK or the optional MX MERCURY. MX LOCK is designed to ensure security for email containing the government agency's or company's confidential information and can proffer either automatic or selective security enforcement. Meanwhile, MX MERCURY manages incoming email with customizable content blocking and filtering in addition to an antivirus program. Importantly, MX MERCURY includes the company's Artificial Intelligence (AI) probabilistic reasoning engine (EPRE), touted to provide 99.95% or higher accuracy in email filtering.

FIPS 140-1, 140-2, and 197 compliant, the Interceptor guarantees the U.S. government's highest security standards, with the MX LOCK-enabled version transforming the sender's email data into unintelligible ciphertext, which is then converted into its original form once it reaches the receiver's side – once the receiver's unique credentials are presented. Another plus of Interceptor is validated records of email receipt including which IP address a given email was accessed from, as well as server locale and attachments' file names. Clearly, this function can assist in GLBA or other policy compliance. MX LOCK versions also allow IT to assign blanket security or to craft security profiles for each user. Five models of Interceptor are available, including the 250 Series (pictured), 250R Series, 500 Series, 1000 Series, and 5000 Series – a lot of choices for some serious email security.

Espion International, Inc. • www.espionintl.com • www.mil-embedded.com/p46276

Editor's Choice Products are drawn from OSM's product database and press releases. Vendors may add their new products to our website at http://submit.opensystemsmedia.com and submit press releases at http://submit.opensystemsmedia.com. OSM reserves the right to publish products based on editors' discretion alone and does not guarantee publication of any product entries.

Neighborhood watch: CPU vendors lock in security

By Chris A. Ciufo, Editor

Mentor Graphics recently asked me to present a keynote speech at their conference on embedded safety and security. The company's position is that outside the realm of DO-178B/254 (software/hardware) for avionics, or NIAP-certified MILS/MLS in certain defense applications, the general embedded market doesn't pay diddly attention to security. My contact at Mentor defines "security" as: protecting key data in bank transactions or medical records, making sure that data at-rest or on-the-fly is unaltered from its originator's intentions, and verifying that systems operate as they were intended without any intervention by bad actors or intentional malware[1]. For the purposes of Mentor's venue, safety was similarly lumped in, though Robert Dewar, president of Ada software company AdaCore, correctly defines "safety" as a system that always works lest it lead to loss of life such as in an aircraft or petroleum refinery.

Be it safety or security, most embedded systems ain't got it. Software, board, and systems designers give scant attention to these topics, as evidenced by how easily hackers broke into Predator UAV video feeds; the example of how Estonia, "the most wired country in Europe," had its banks shut down in 2007 by hackers; or possibly even the unexplained acceleration on some Toyotas, which some pundits say might have been something intentionally created by an outsider. Rather than leave safety and security to chance, both Freescale and Intel are putting big effort into their silicon and related ecosystems with new features, instructions, and logic blocks. And boy, am I impressed with their efforts.

Freescale cries "uncle" for AltiVec

As we went to press in late September, Freescale announced that AltiVec technology would be added into P3, P4, and P5 QorIQ multicore processors over the next several months. On the surface, the popular AltiVec SIMD vector processor has nothing directly to do with safety or security, but the QorIQ platform's Trust Architecture (TA) is extremely comprehensive and impressive at securing embedded systems. In military applications, the QorIQ has been a real dud follow-on to the popular MPC74xx PowerPC CPUs with AltiVec, causing mil designers instead to flock to Intel's x86s in Core 2 Duos, Xeons, and Core i5/i7 CPUs. I'm betting that putting AltiVec into QorIQ will at last give a road map to legacy PowerPC designs and slow Intel's socket-stealing Blitzkrieg. If this happens, the Trust Architecture becomes a hugely significant addition to next-gen DoD designs and COTS single board computers.

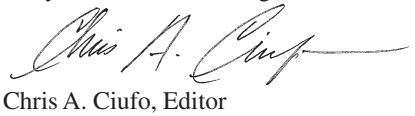
The Trust Architecture uses a secure-boot feature to bring up the system in a known (and trusted) state, then maintains that during runtime. Designers can be confident that the software initially loaded into the system or during updates is as-expected. Freescale added functional blocks to the QorIQ to protect against: 1. *Theft of functionality,* where legitimate users lose control; 2. *Theft of third-party data* – to an unauthorized party; and 3. *Theft of uniqueness,* via reverse engineering or duplication. The multicore CPU can boot securely from onboard memory enabled by a fuse, and can even utilize an onboard hypervisor to virtualize all the CPU's cores, not just the e500mc-vcpu virtual boot-up logic. There's even an "X" bit in the TLB that controls whether a memory page's contents can be executable instructions[2]. The architecture is complicated and more than I want to cover here, but the features in the TA fill 23 pages in Freescale's *An Introduction to the QorIQ Platform's Trust Architecture.* DoD designers will want to take a second look now that AltiVec is on the way.

Intel, McAfee, and Embedded

At the recent Intel Developer Forum (IDF), CEO Paul Otellini made it clear in the opening keynote that one of Intel's three Pillars of Computing is Security, in a world of always-on computing, "20 billion" mobile Internet devices, and an increasingly unsafe world of targeted security breaches and organized crime-based hacks. The company just did its biggest acquisition ever: the $7.6 billion purchase of anti-virus company McAfee.

Not much was said pertaining to McAfee during IDF, though Doug Davis, VP/GM of the Embedded Communications Group, responded to an audience question by stating that McAfee can work with antitheft software such as LoJack that can "brick" and locate your laptop, although the (future) approach is to "block Day Zero attacks." He said that the whole raft of existing Intel silicon security features such as VT, vPro, TXT, and so on "can be used in a whole different way … wait for 2011." The plan for the Security pillar is to lower the number of attack surfaces … whatever that means. By the way, you might piece together Intel's security strategy by checking out the technical session "Securing Today's Data Centers Against Tomorrow's Attacks." I doubt that Intel is going to create a killer QorIQ Trust Architecture since that's not the company's focus. Instead, they'll add chip-enabled data center features (vPro and VT) with existing instructions to balance on-chip security with McAfee-like desktop security running in the OS[3].

It's heartening that even if designers haven't yet taken security or safety seriously, these two CPU vendors will. That means they'll form their own neighborhood watch and be on guard in everyone's embedded neighborhood.



Chris A. Ciufo, Editor
cciufo@opensystemsmedia.com

[1] Mentor and all software companies distinguish code or systems intentionally tampered with from systems that are merely behaving badly due to poorly written, verified, or tested code. In the latter, static and dynamic analysis tools are used to make sure the system operates as expected in all operational modes.
[2] This predates Intel's x86 NX bit (No execute) by several *generations*.
[3] I wonder if Wind River's VxWorks will get built-in anti-virus. Intel bought Wind River in 2009.

GE
Intelligent Platforms

You can only target what you can track.

As the deployment of unmanned vehicles has increased, so has the demand for high-performance video tracking capabilities. In response, GE Intelligent Platforms has developed a full range of cutting-edge, real-time COTS video tracking, compression and image processing technology that is ruggedized and low power.

We support simultaneous compression of multiple channels of high-resolution video in rugged environments. Simply connect your video inputs and begin streaming HD at full frame rates for superb tracking performance and reduced operator workload. No additional integration or software development is required.

For more information, visit:
www.ge-ip.com/image-processing

imagination at work

DEFY SIZE, WEIGHT AND POWER

YOUR TOTAL SOLUTIONS PARTNER

Photo courtesy of Northrop Grumman

Signal & Image Processing

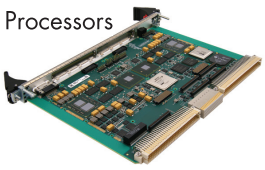
FPGAs

VPX3-450

Radar Processing

Digital Signal Processors

CHAMP-AV5



Flight Control

Multi-Platform Mission Computers

MPMC-9350 & MPMC-9310 (VPX, VME or CompactPCI®)

Do you need innovative solutions or complete integration services for high-density data processing, with optimized I/O and limited size, weight and power (SWaP) requirements? From board-level products to fully integrated systems, we provide leading-edge OpenVPX™ solutions enabling you to defy your SWaP challenges in the most rugged operating conditions. Speed your time-to-market and lower your development costs with our COTS products or modified COTS (MCOTS) and engineering services. **Ask your representative about the new VPX system specification, OpenVPX.**

Data Management

Rugged NAND Flash Storage

XMC/PMC-550

System Connectivity

Secure Ethernet Routers

VPX3-685 Fireblade

Command & Control

Single Board Computers

VPX3-127 & VPX3-1252

CURTISS WRIGHT Controls Embedded Computing

sales@cwcembedded.com

cwcembedded.com

BOARDS & SYSTEMS ABOVE & BEYOND